1/40

Fig.1

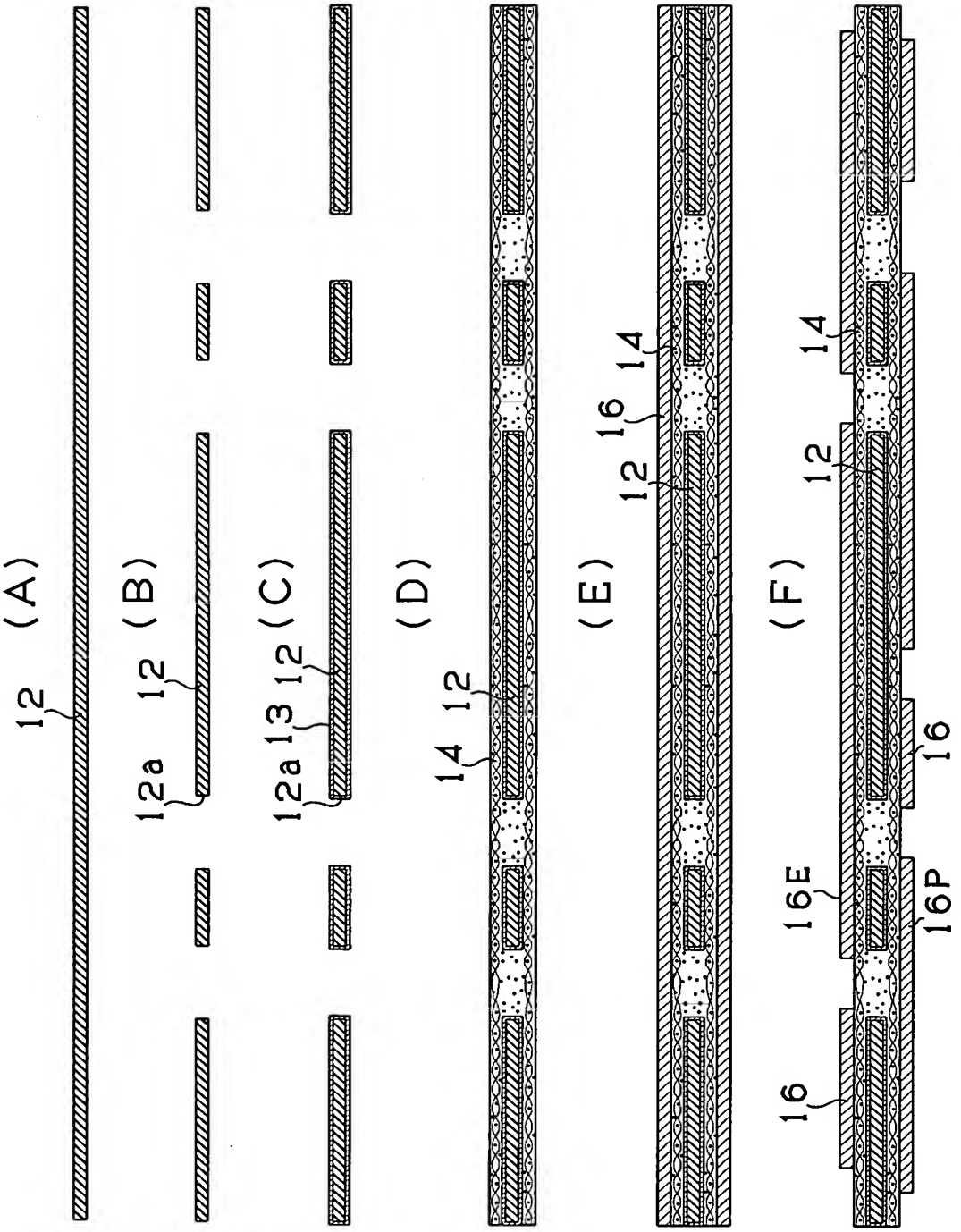


Fig.2

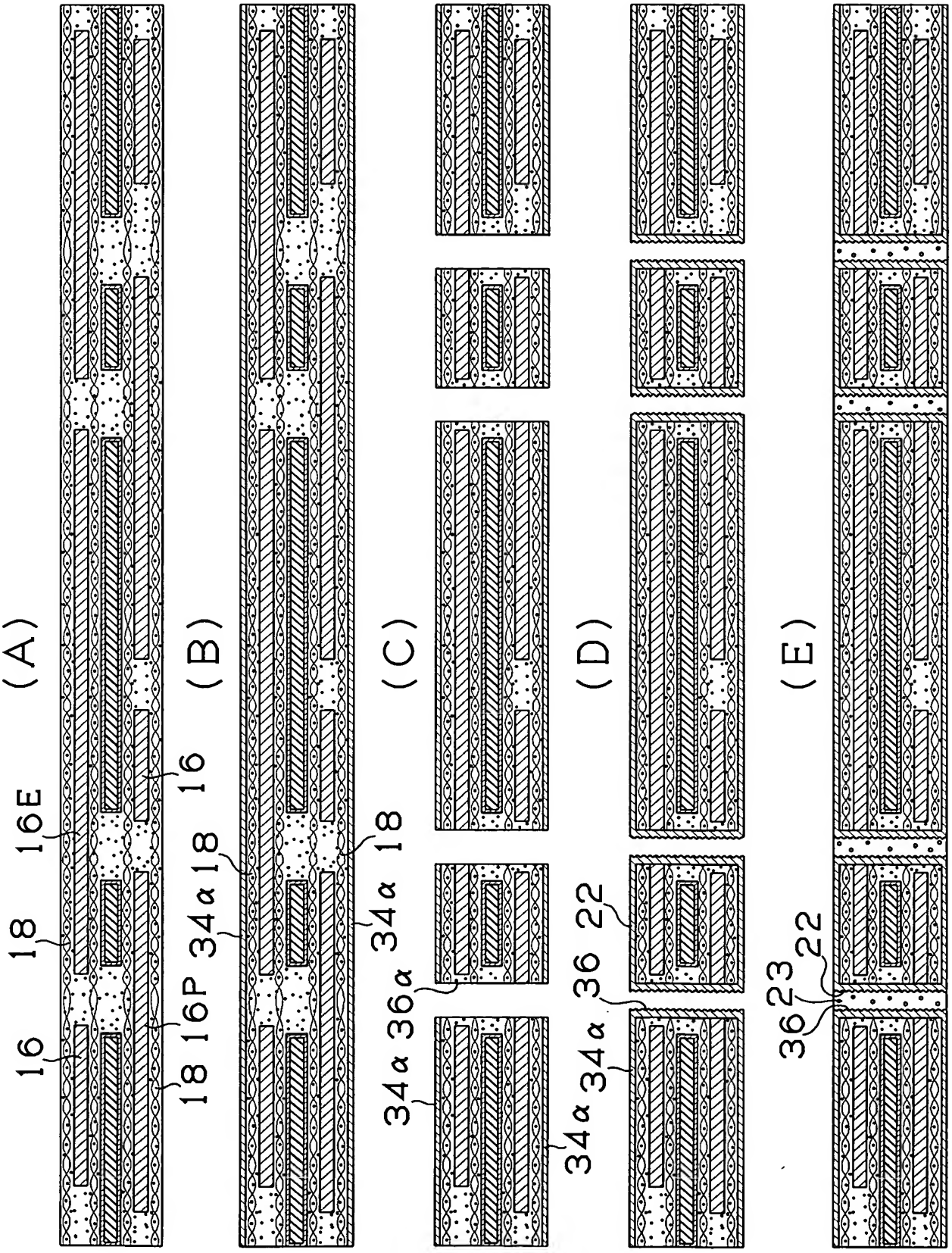

(A)
(B)
(C)
(D)
(E)
16
18
16E
18 16P
16
34α 18
34α 18
34α 36α
34α 36α
34α
36 22
22
23
36

Fig.3

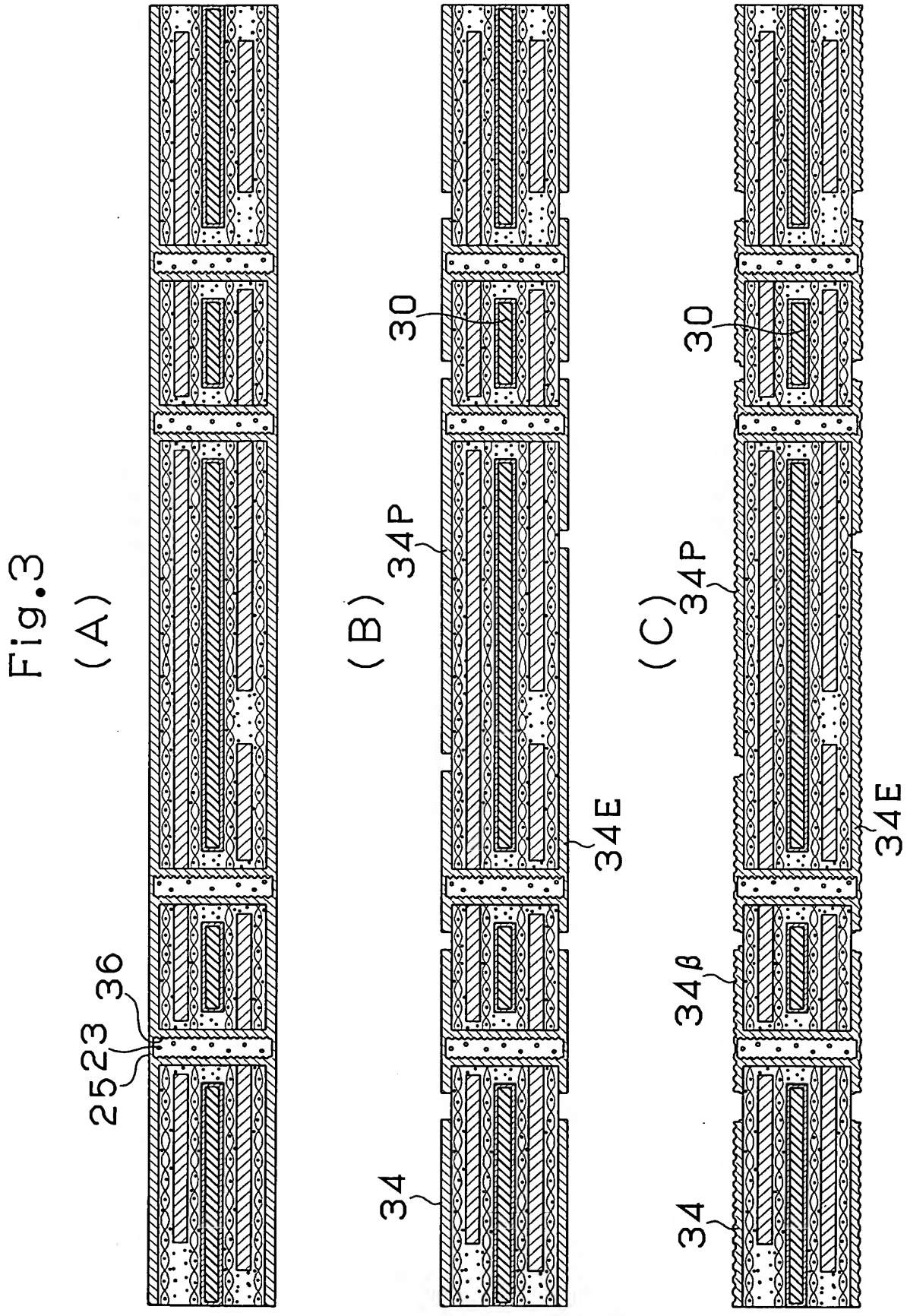
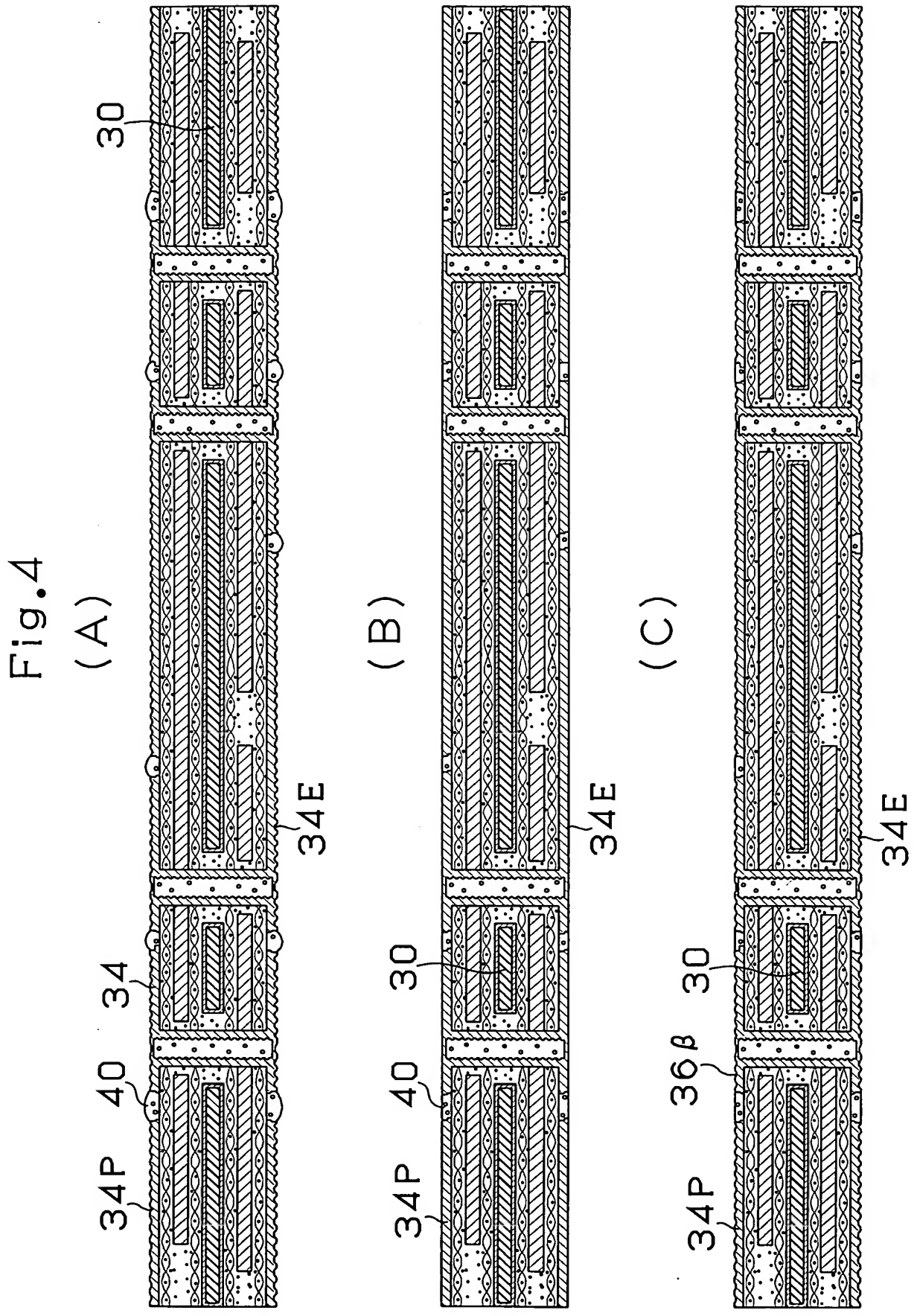


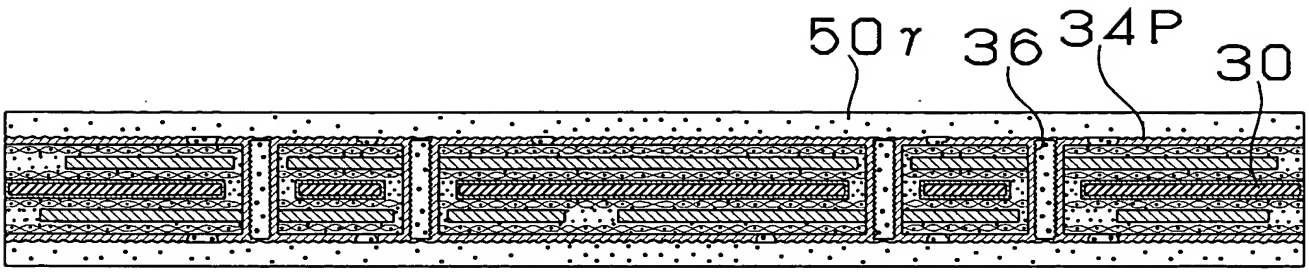
Fig.4



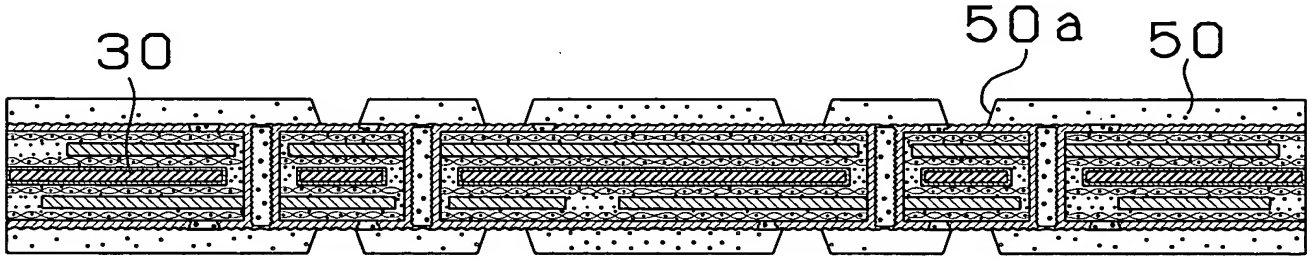
5/40

Fig.5

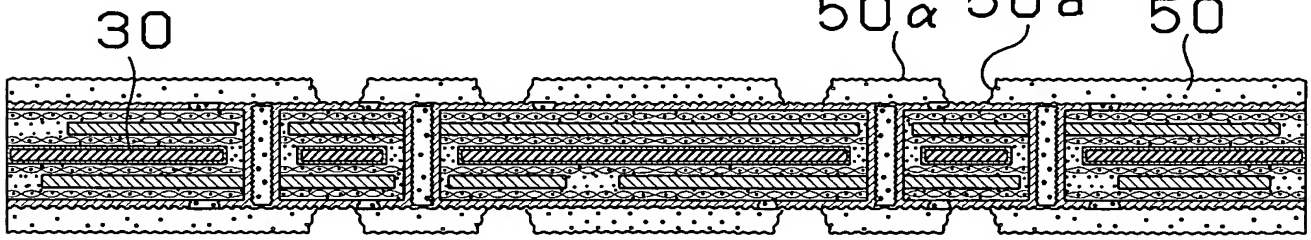
(A)



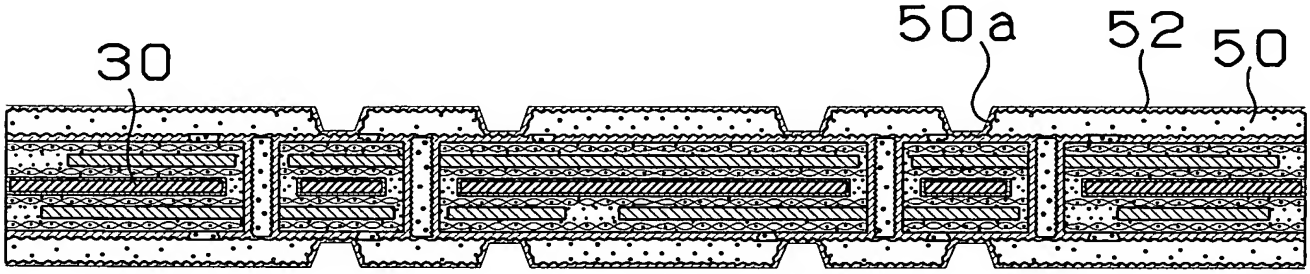
(B)



(C)



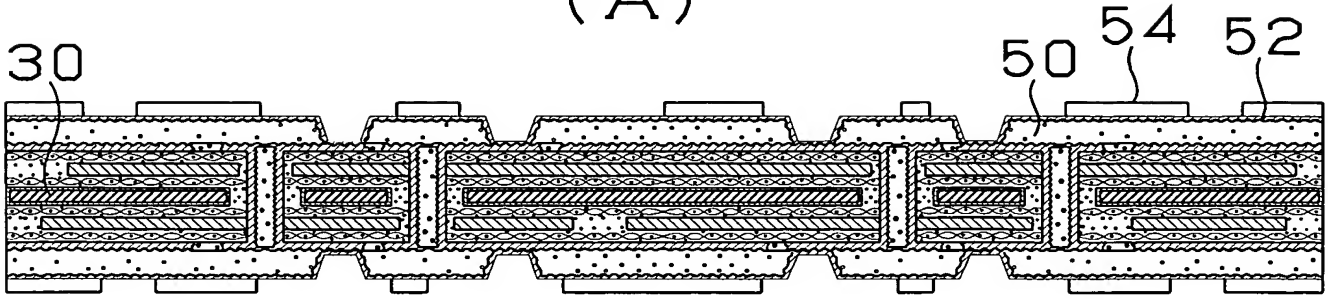
(D)



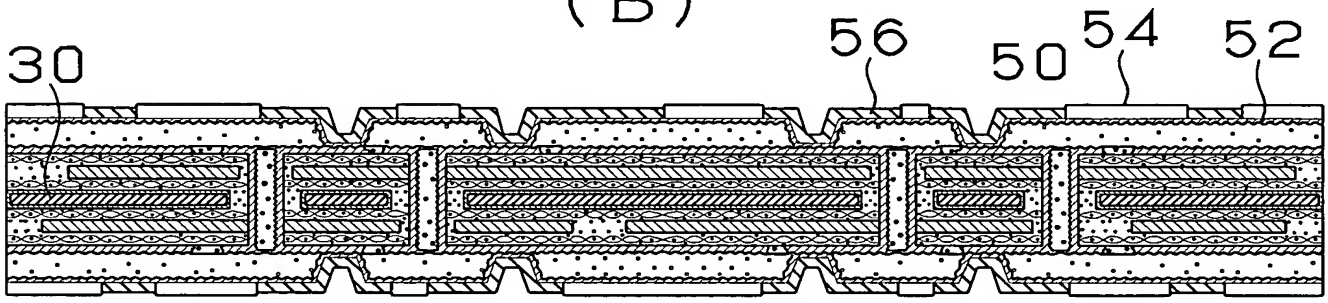
6/40

Fig.6

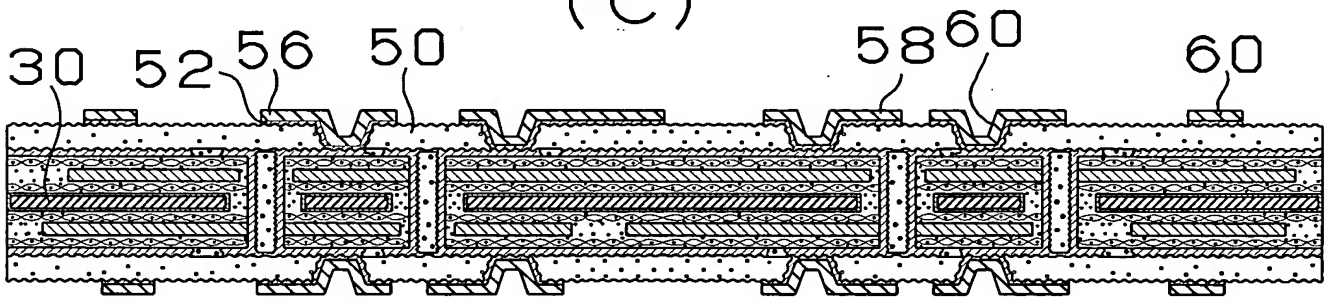
(A)



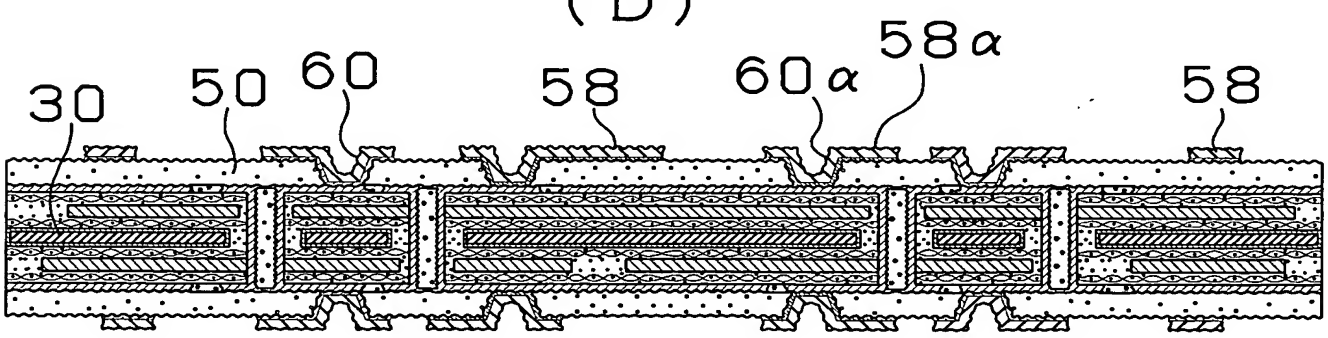
(B)



(C)



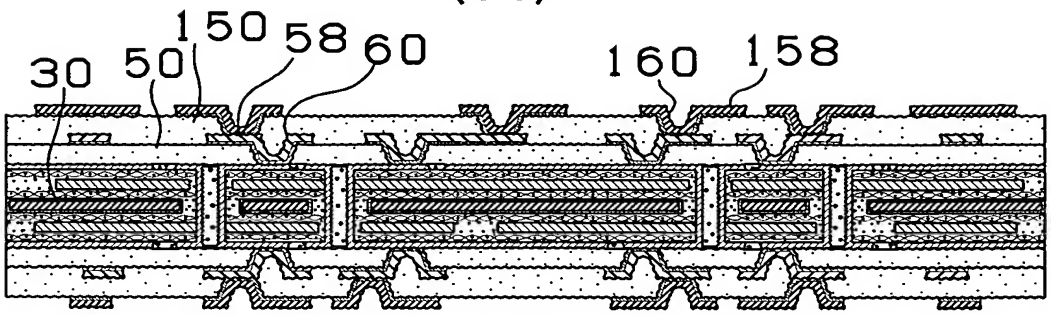
(D)



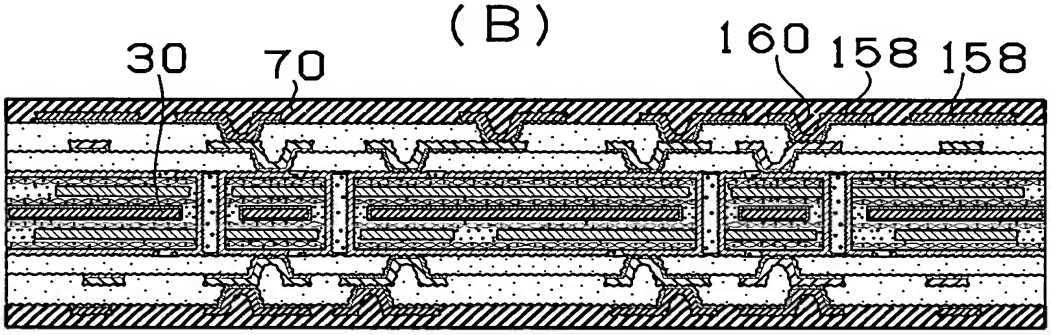
7/40

Fig.7

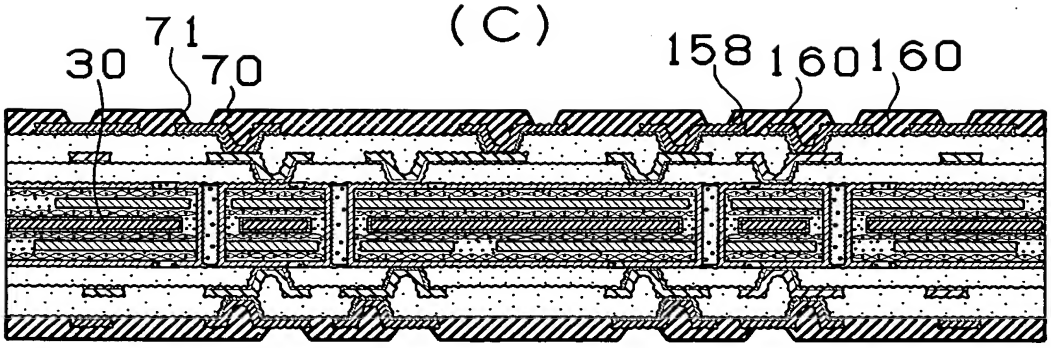
(A)



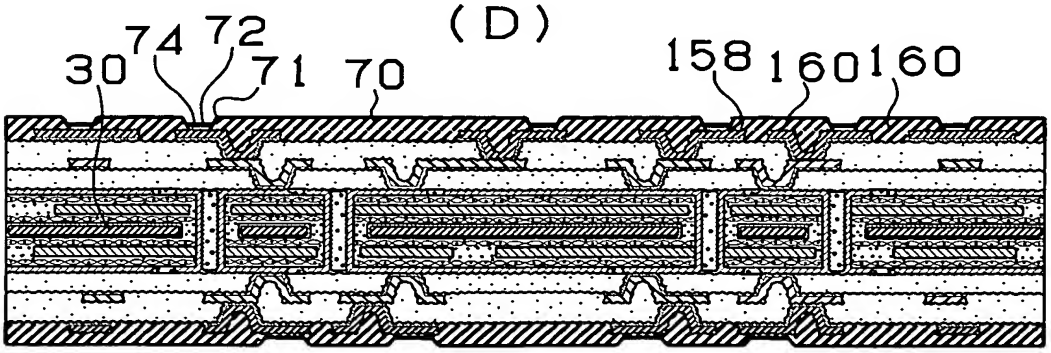
(B)



(C)



(D)



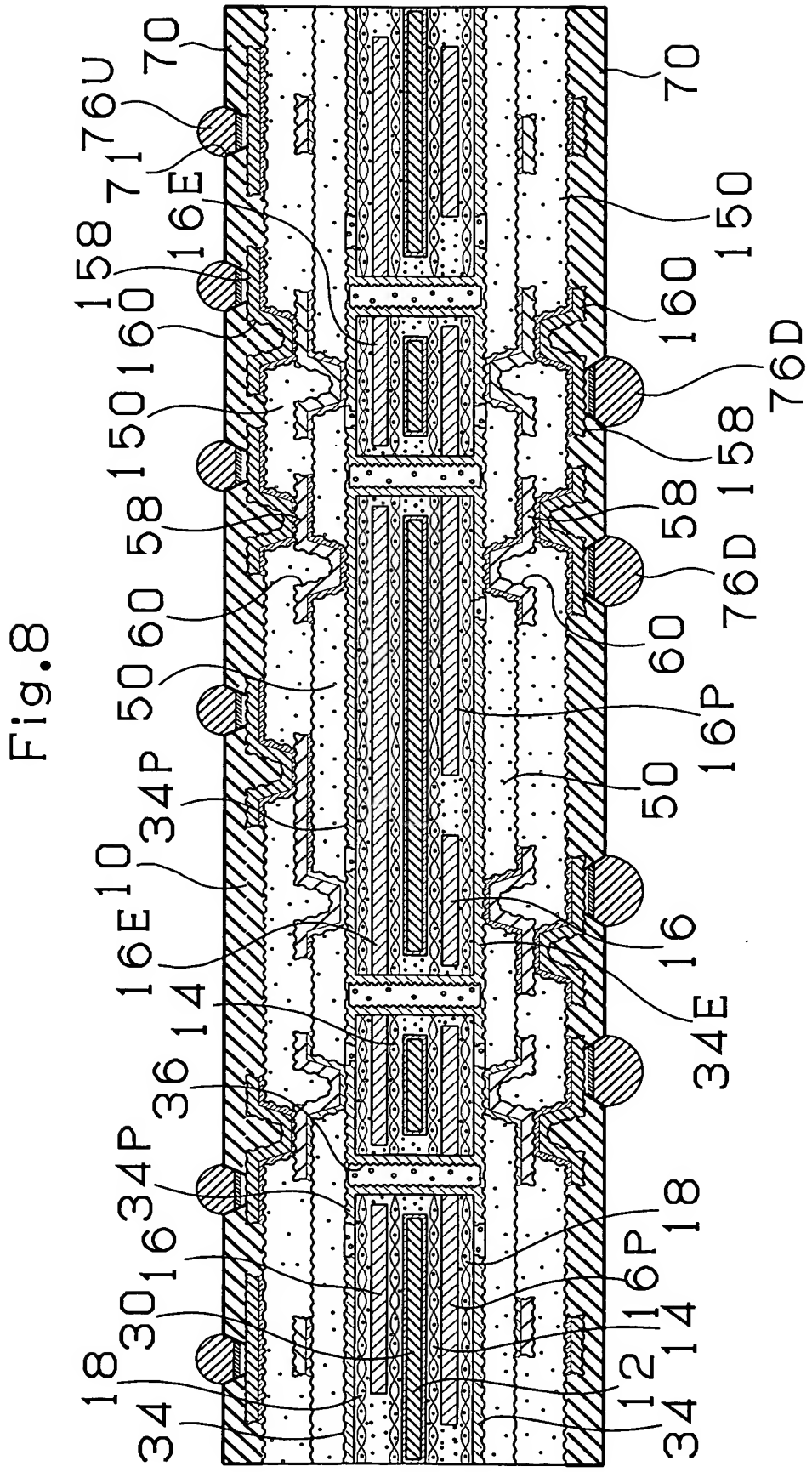

70
76U
71
16E
158
160
150
58
60
50
34P
10
16E
14
36
34P
16
30
18
34
70
150
160
76D
158
58
76D
60
16P
50
16
34E
18
16P
14
12
34

Fig.8

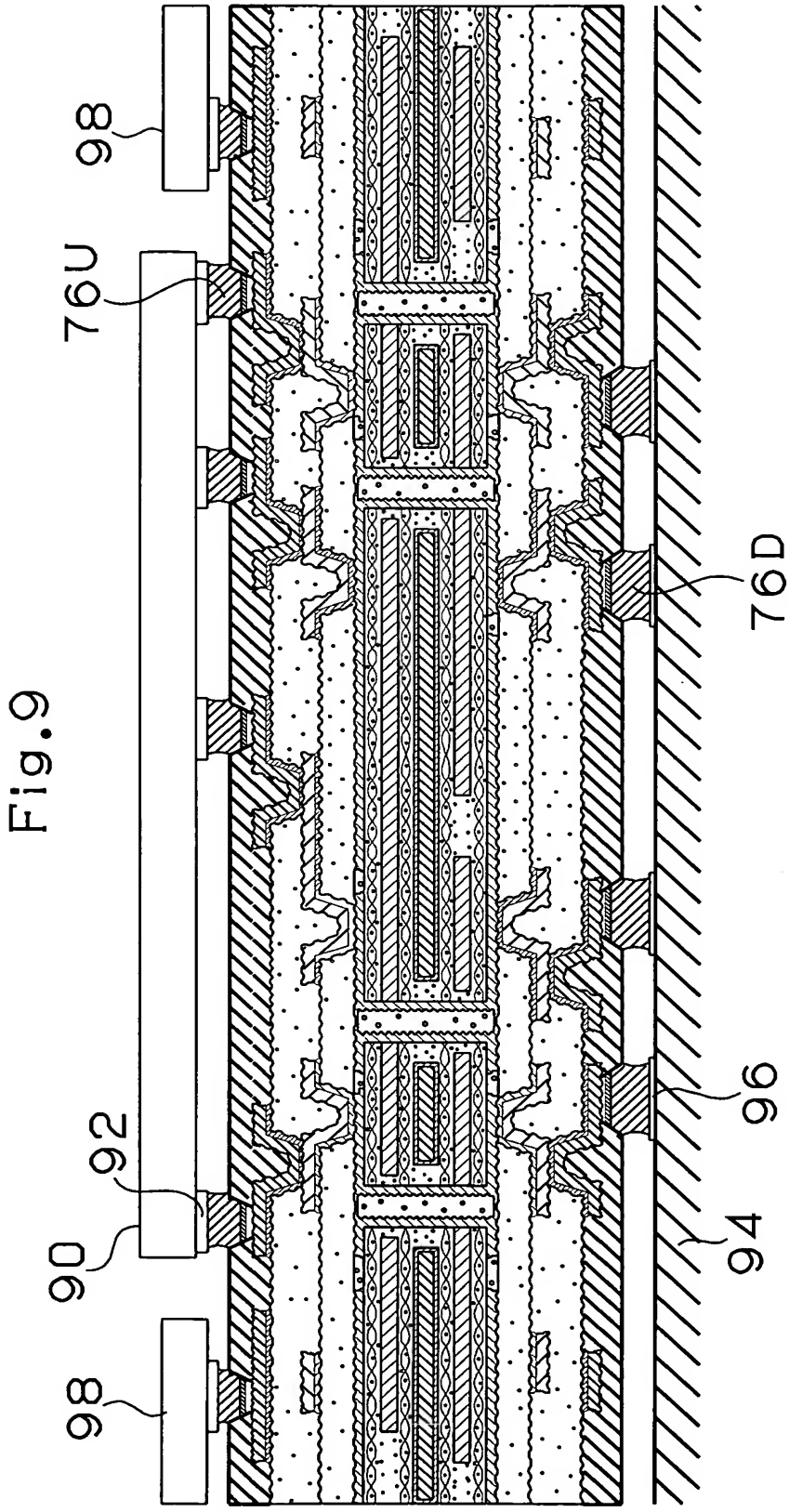


Fig.9

Fig.10

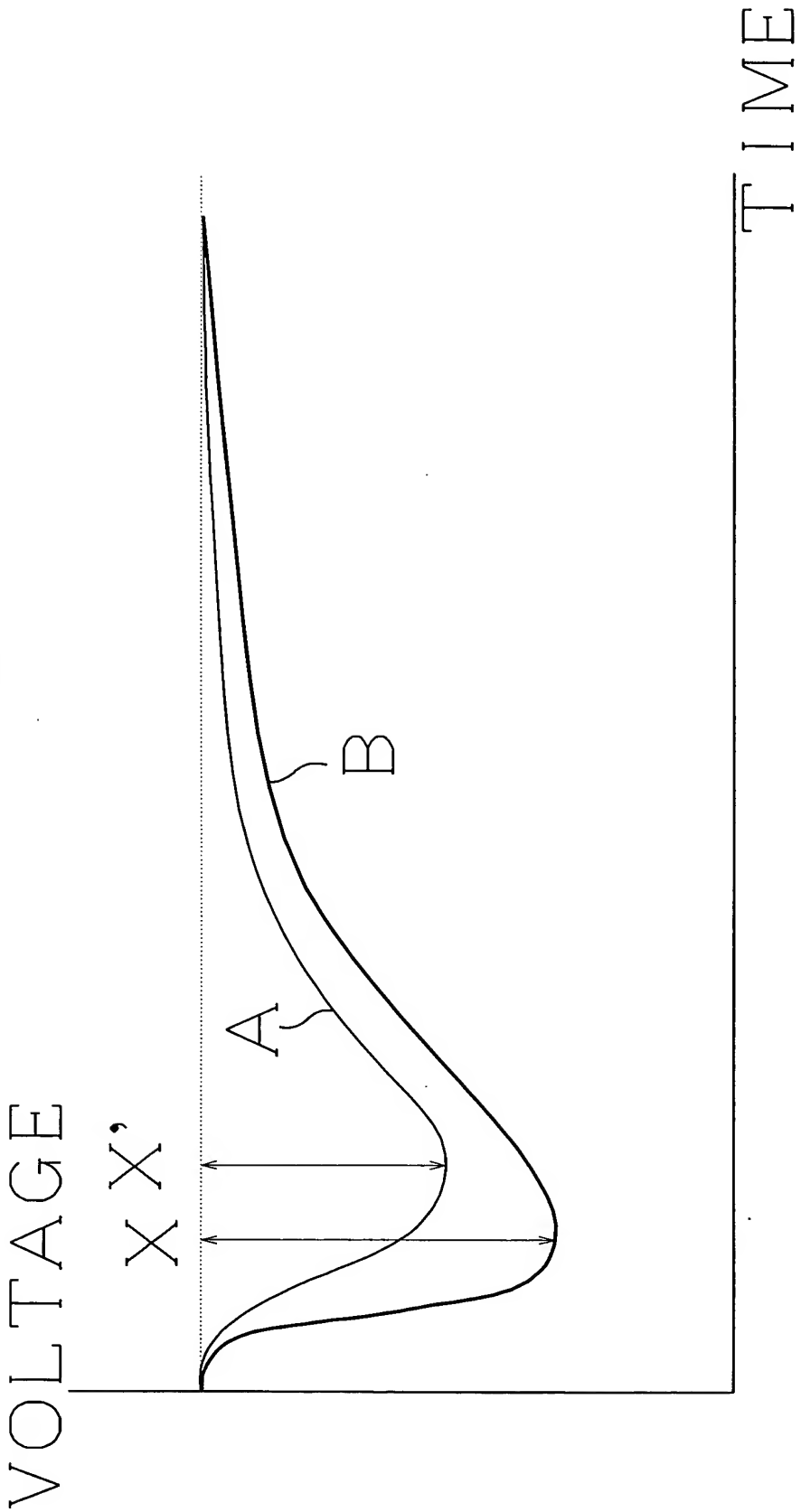


Fig.11

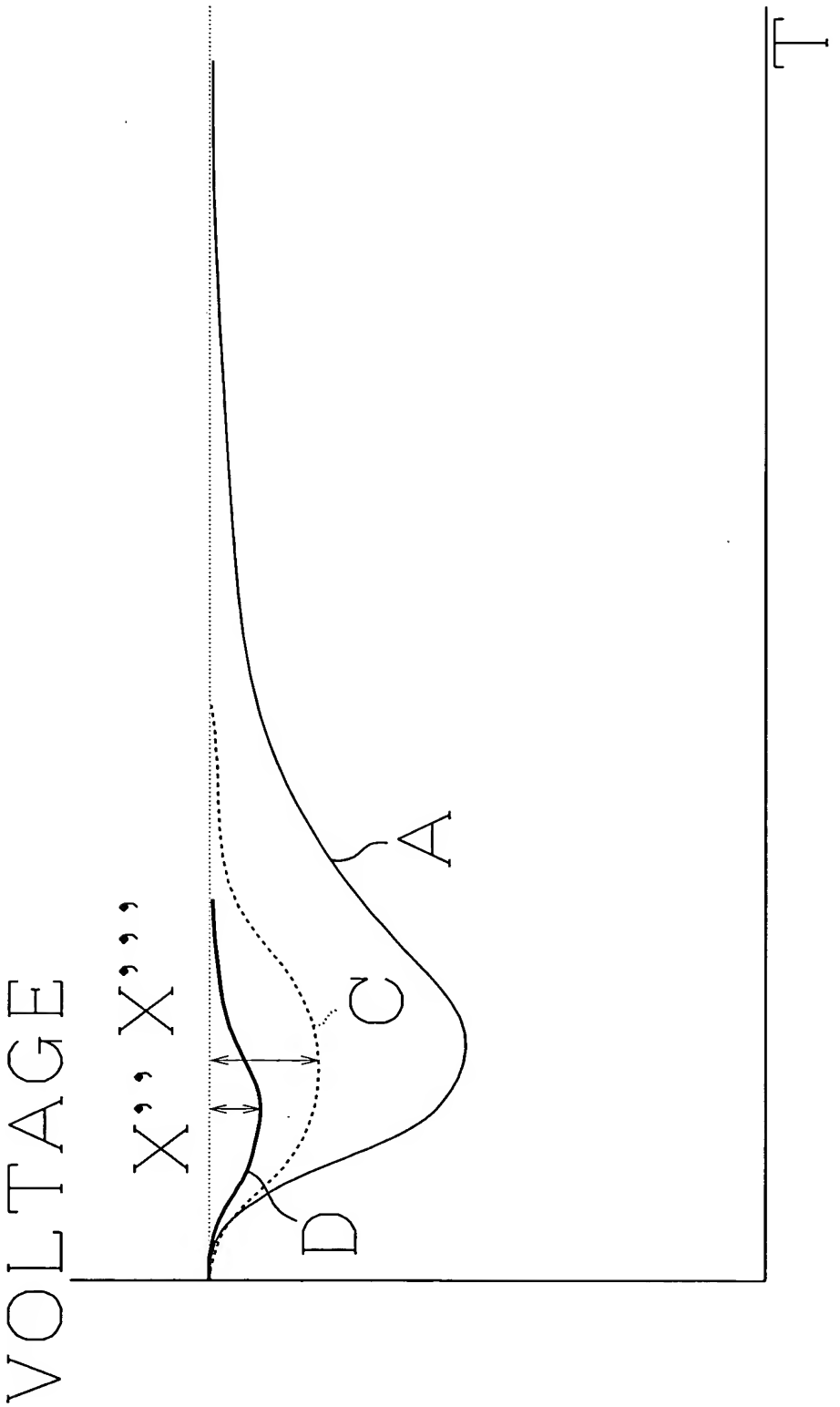


Fig.12

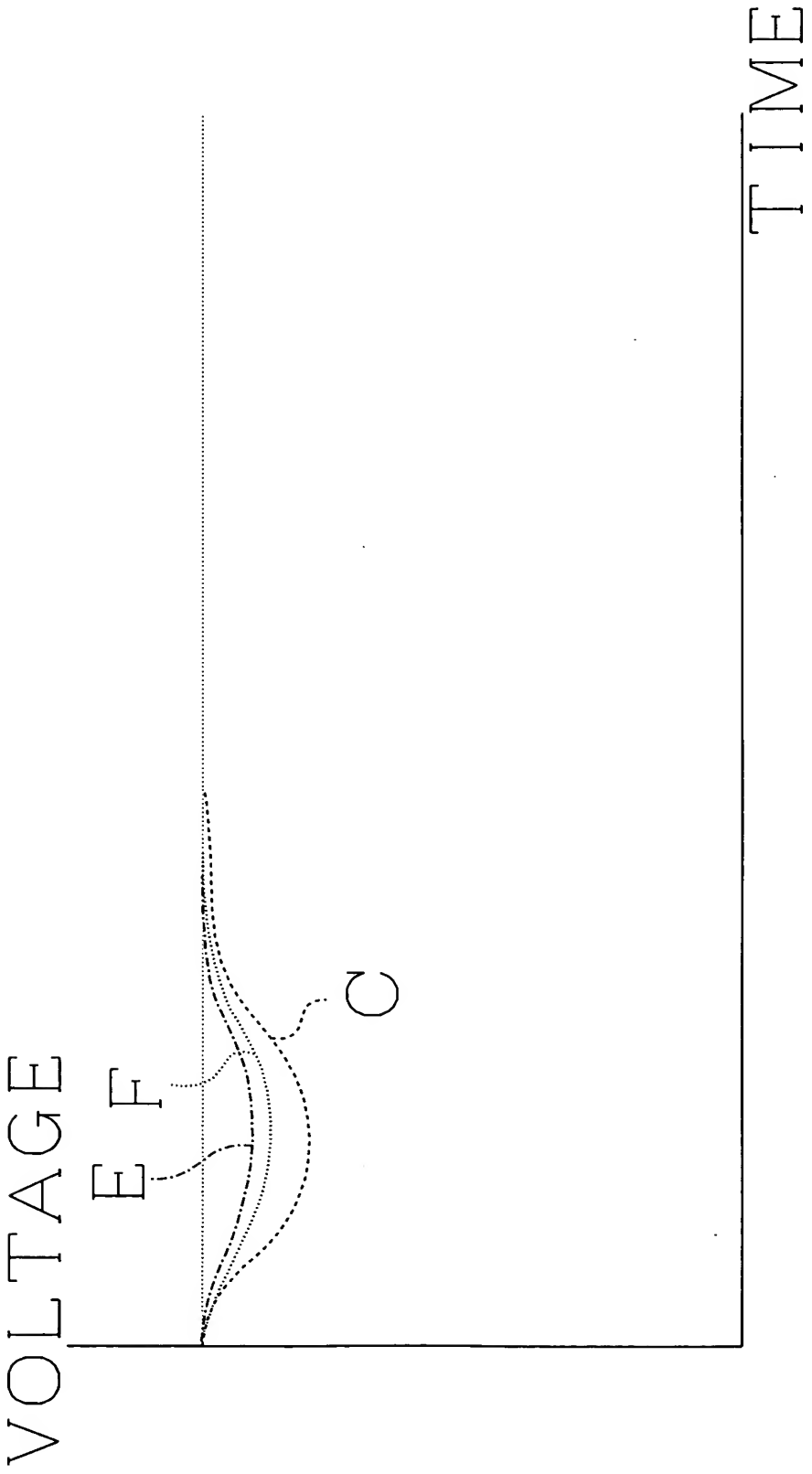


Fig.13

#	α1／α2	QUANTITY OF LAYERS IN INNER LAYER	THICKNESS OF CONDUCTIVE LAYER ON INTERLAYER INSULATION LAYER (μm)	THICKNESS OF POWER SOURCE LAYER ON FRONT SURFACE LAYER OF CORE SUBSTRATE (μm)	THICKNESS OF POWER SOURCE LAYER IN INNER LAYER OF CORE SUBSTRATE (μm)	SUM OF THICKNESSES OF POWER SOURCE LAYERS OF CORE (μm)	AMOUNT OF VOLTAGE DROP (V)	RESULT OF HAST TEST
FIRST EMBODIMENT－1	2	2	20	15	25	40	0.091	○
FIRST EMBODIMENT－2	1.2	2	20	9	15	24	0.093	○
FIRST EMBODIMENT－3	3	2	20	15	45	60	0.085	○
FIRST EMBODIMENT－4	3.75	2	20	15	60	75	0.085	○
FIRST EMBODIMENT－5	30.75	12	20	15	100	615	0.095	○
FIRST EMBODIMENT－6	40.75	16	20	15	100	815	0.097	○
FIRST EMBODIMENT－7	3	2	20	45	15	60	0.087	○
FIRST EMBODIMENT－8	3.75	2	20	60	15	75	0.086	○
FIRST EMBODIMENT－9	3.25	2	20	15	50	65	0.084	○
FIRST EMBODIMENT－10	8.25	2	20	15	150	165	0.083	○
FIRST EMBODIMENT－11	9.5	2	20	15	175	190	0.09	×
FIRST EMBODIMENT－12	10.75	2	20	15	200	215	0.093	×
FIRST EMBODIMENT－28	7	2	20	15	125	140	0.084	○
FIRST COMPARATIVE EXAMPLE －1	1	2	20	10	10	20	0.108	○
FIRST COMPARATIVE EXAMPLE－2	42	16	20	40	100	840	0.103	○
FIRST COMPARATIVE EXAMPLE－3	50.75	20	20	15	100	1015	0.123	○

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Fig.14

#	WIDTH OF CONDUCTOR/INTERVAL OF CONDUCTORS(μm)				
	5/5	7.5/7.5	10/10	12.5/12.5	15/15
FIRST EMBODIMENT—3	○	○	○	○	○
FIRST EMBODIMENT—4	○	○	○	○	○
FIRST EMBODIMENT—7	×	×	○	○	○
FIRST EMBODIMENT—8	×	×	○	○	○

Fig.15

#	α1／α2	QUANTITY OF LAYERS IN INNER LAYER	THICKNESS OF CONDUCTIVE LAYER ON INTERLAYER INSULATION LAYER (μm)	THICKNESS OF POWER SOURCE LAYER ON FRONT SURFACE LAYER OF CORE SUBSTRATE (μm)	THICKNESS OF POWER SOURCE LAYER IN INNER LAYER OF CORE SUBSTRATE (μm)	SUM OF THICKNESSES OF POWER SOURCE LAYERS OF CORE (μm)	AMOUNT OF VOLTAGE DROP (V)	PRESENCE/ABSENCE OF MALFUNCTION		
								No.1 IC MOUNTED	No.2 IC MOUNTED	No.3 IC MOUNTED
FIRST EMBODIMENT−1	2	2	20	15	25	40	0.091	NONE	YES	YES
FIRST EMBODIMENT−2	1.2	2	20	9	15	24	0.093	NONE	YES	YES
FIRST EMBODIMENT−3	3	2	20	15	45	60	0.085	NONE	NONE	NONE
FIRST EMBODIMENT−4	3.75	2	20	15	60	75	0.085	NONE	NONE	NONE
FIRST EMBODIMENT−5	30.75	12	20	15	100	615	0.095	NONE	YES	YES
FIRST EMBODIMENT−6	40.75	16	20	15	100	815	0.097	NONE	YES	YES
FIRST EMBODIMENT−7	3	2	20	45	15	60	0.087	NONE	NONE	YES
FIRST EMBODIMENT−8	3.75	2	20	60	15	75	0.086	NONE	NONE	YES
FIRST EMBODIMENT−9	3.25	2	20	15	50	65	0.084	NONE	NONE	NONE
FIRST EMBODIMENT−10	8.25	2	20	15	150	165	0.083	NONE	NONE	YES
FIRST EMBODIMENT−11	9.5	2	20	15	175	190	0.09	NONE	YES	YES
FIRST EMBODIMENT−12	10.75	2	20	15	200	215	0.093	NONE	YES	YES
FIRST EMBODIMENT−27	4	4	20	15	32.5	80	0.087	NONE	NONE	YES
FIRST EMBODIMENT−28	7	2	20	15	125	140	0.084	NONE	NONE	NONE
FIRST COMPARATIVE EXAMPLE−1	1	2	20	10	10	20	0.108	YES	YES	YES
FIRST COMPARATIVE EXAMPLE−2	42	16	20	40	100	840	0.103	YES	YES	YES
FIRST COMPARATIVE EXAMPLE−3	50.75	20	20	15	100	1015	0.123	YES	YES	YES

Fig.16

#	α1 / α2	HAVING NO DUMMY LAND TH%	QUANTITY OF LAYERS IN INNER LAYER	THICKNESS OF CONDUCTIVE LAYER ON INTERLAYER INSULATION LAYER (μm)	THICKNESS OF POWER SOURCE LAYER ON FRONT SURFACE LAYER OF CORE SUBSTRATE (μm)	THICKNESS OF POWER SOURCE LAYER IN INNER LAYER OF CORE SUBSTRATE (μm)	SUM OF THICKNESSES OF POWER SOURCE LAYERS OF CORE (μm)	PRESENCE/ABSENCE OF MALFUNCTION		
								No.1 IC MOUNTED	No.2 IC MOUNTED	No.3 IC MOUNTED
FIRST EMBODIMENT−13	3	50	2	20	15	45	60	NONE	NONE	NONE
FIRST EMBODIMENT−14	3	100	2	20	15	45	60	NONE	NONE	NONE
FIRST EMBODIMENT−15	3.25	50	2	20	15	50	65	NONE	NONE	NONE
FIRST EMBODIMENT−16	3.25	100	2	20	15	50	65	NONE	NONE	NONE
FIRST EMBODIMENT−17	3.75	50	2	20	15	60	75	NONE	NONE	NONE
FIRST EMBODIMENT−18	3.75	100	2	20	15	60	75	NONE	NONE	NONE
FIRST EMBODIMENT−19	8.25	50	2	20	15	150	165	NONE	NONE	NONE
FIRST EMBODIMENT−20	8.25	100	2	20	15	150	165	NONE	NONE	NONE
FIRST EMBODIMENT−21	9.5	50	2	20	15	175	190	NONE	NONE	YES
FIRST EMBODIMENT−22	9.5	100	2	20	15	175	190	NONE	NONE	YES
FIRST EMBODIMENT−23	10.75	50	2	20	15	200	215	NONE	NONE	YES
FIRST EMBODIMENT−24	10.75	100	2	20	15	200	215	NONE	NONE	YES
FIRST EMBODIMENT−25	3	50	2	20	45	15	60	NONE	NONE	YES
FIRST EMBODIMENT−26	3	100	2	20	45	15	60	NONE	NONE	YES
FIRST EMBODIMENT−29	4	50	4	20	15	32.5	80	NONE	NONE	NONE
FIRST EMBODIMENT−30	4	100	4	20	15	32.5	80	NONE	NONE	NONE

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Fig.17

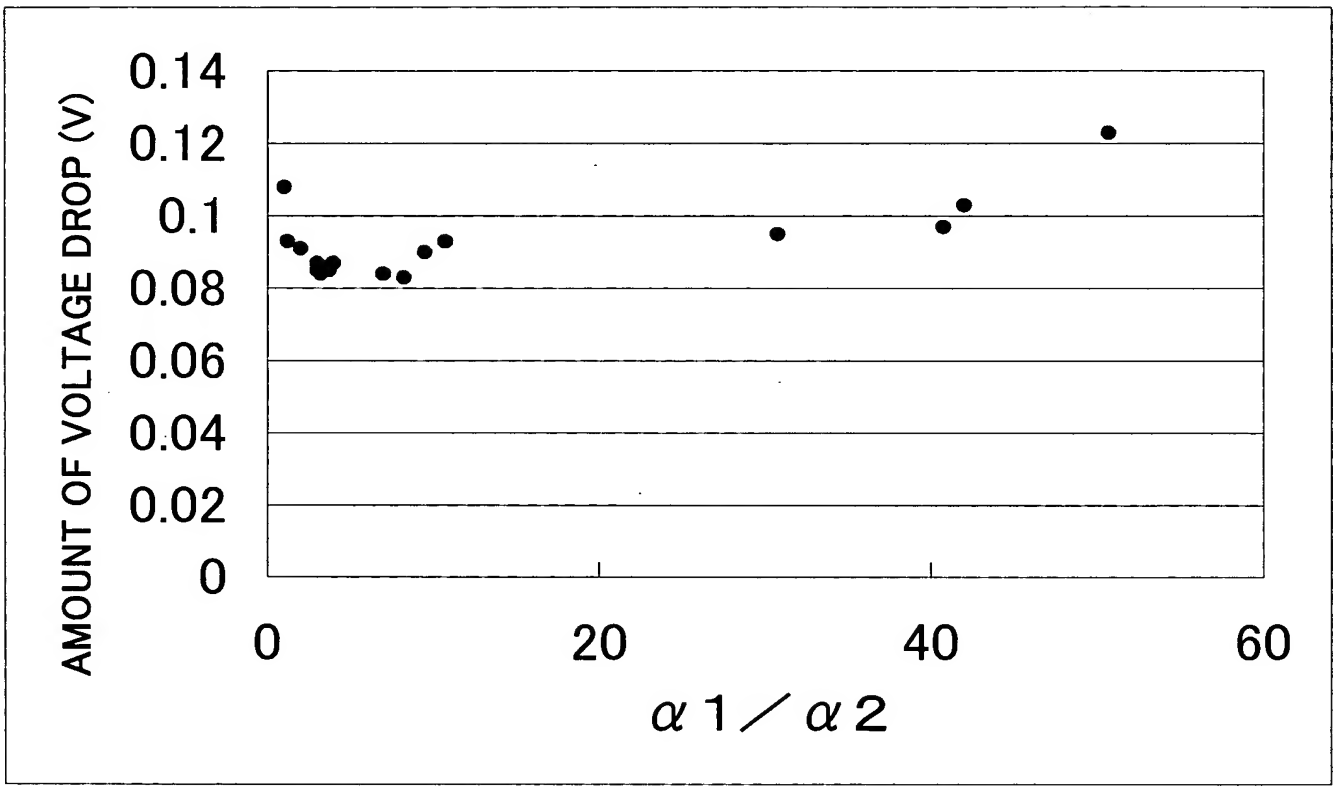
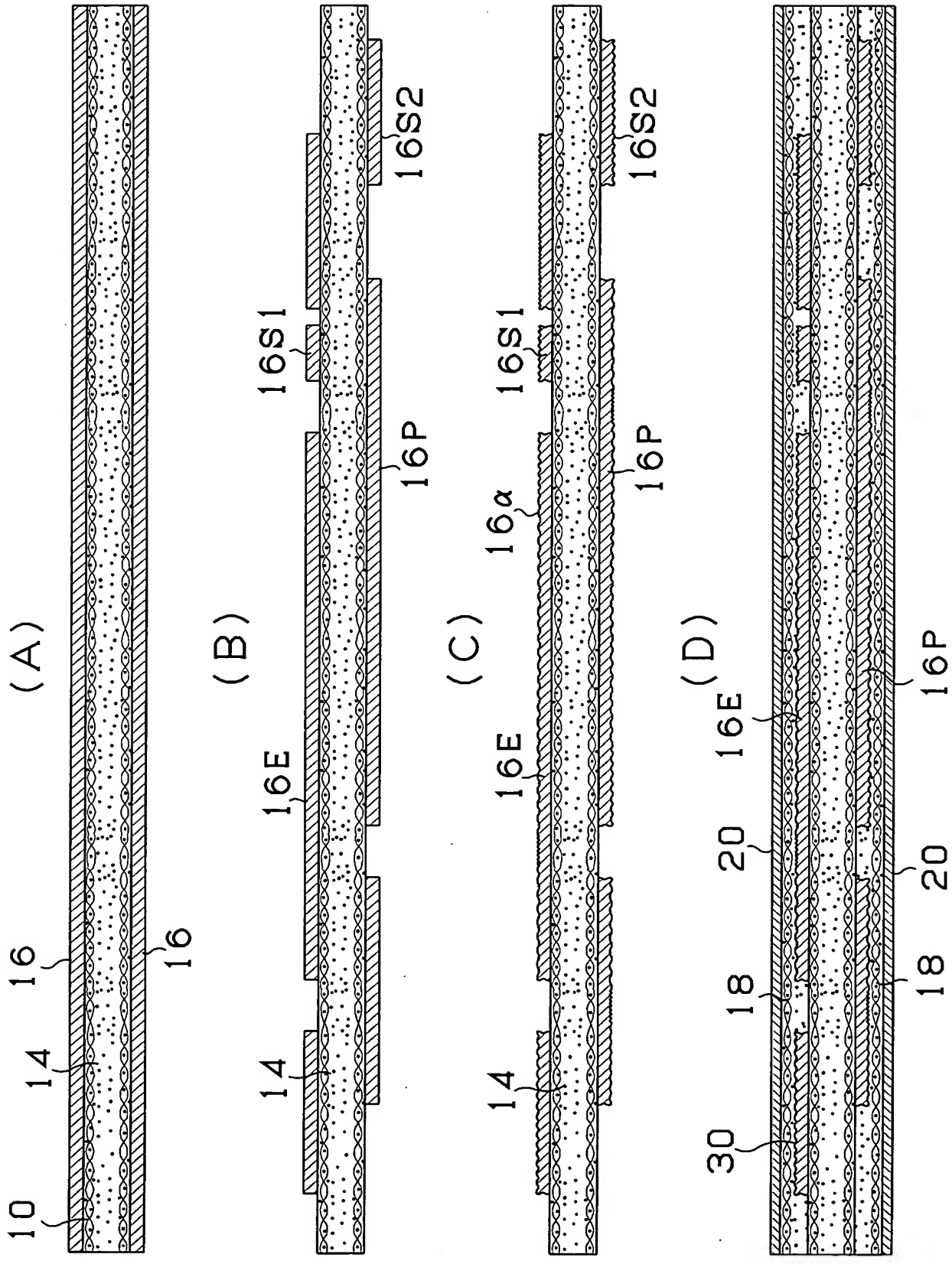

AMOUNT OF VOLTAGE DROP (V)
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
0
20
40
60
α1／α2

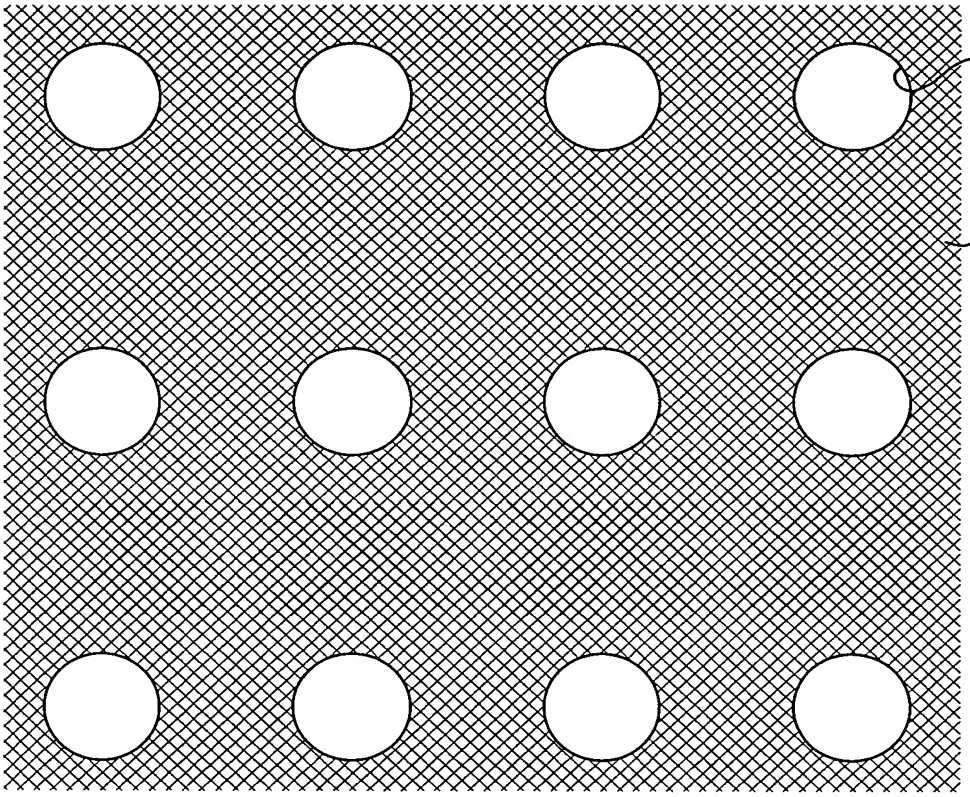
Fig.18


(A)
10
14
16
16
(B)
14
16E
16S1
16P
16S2
(C)
14
16E
16α
16S1
16P
16S2
(D)
30
18
20
16E
16P
18
20

19/40

Fig.19

(A)



(B)

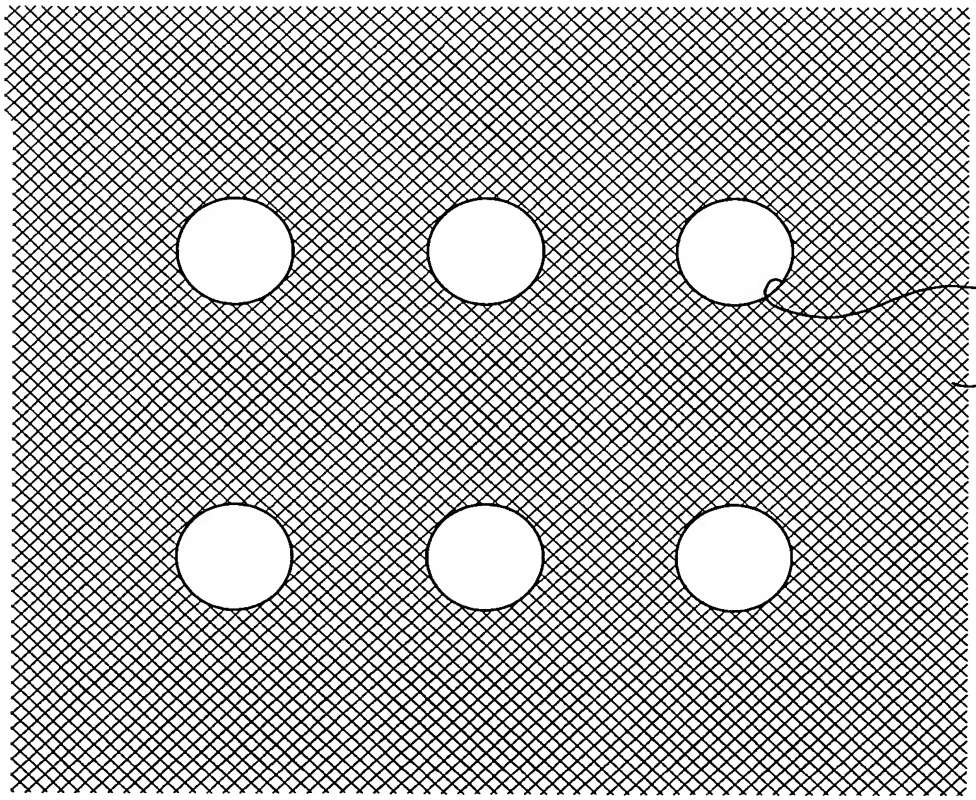


Fig.20

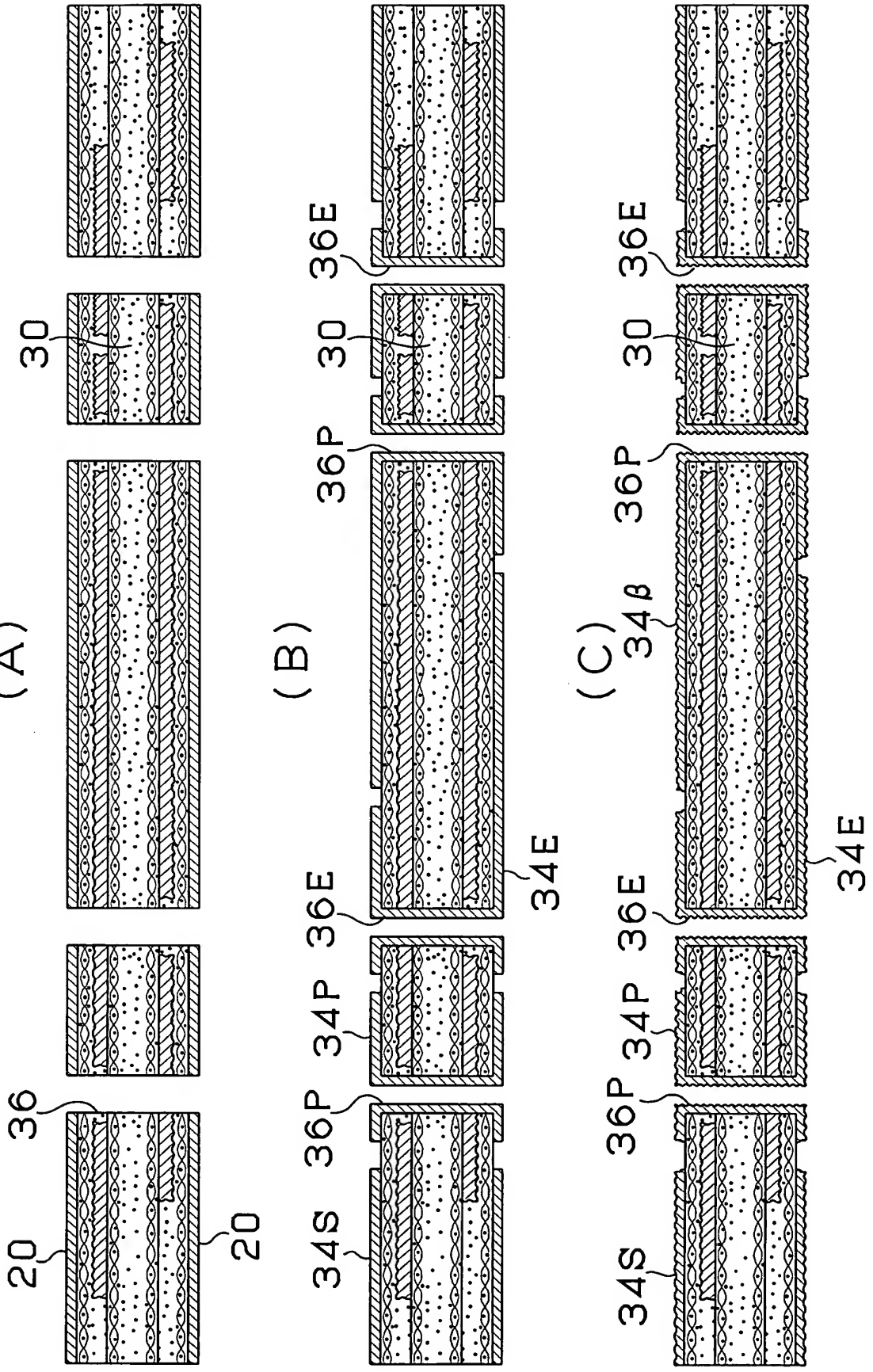
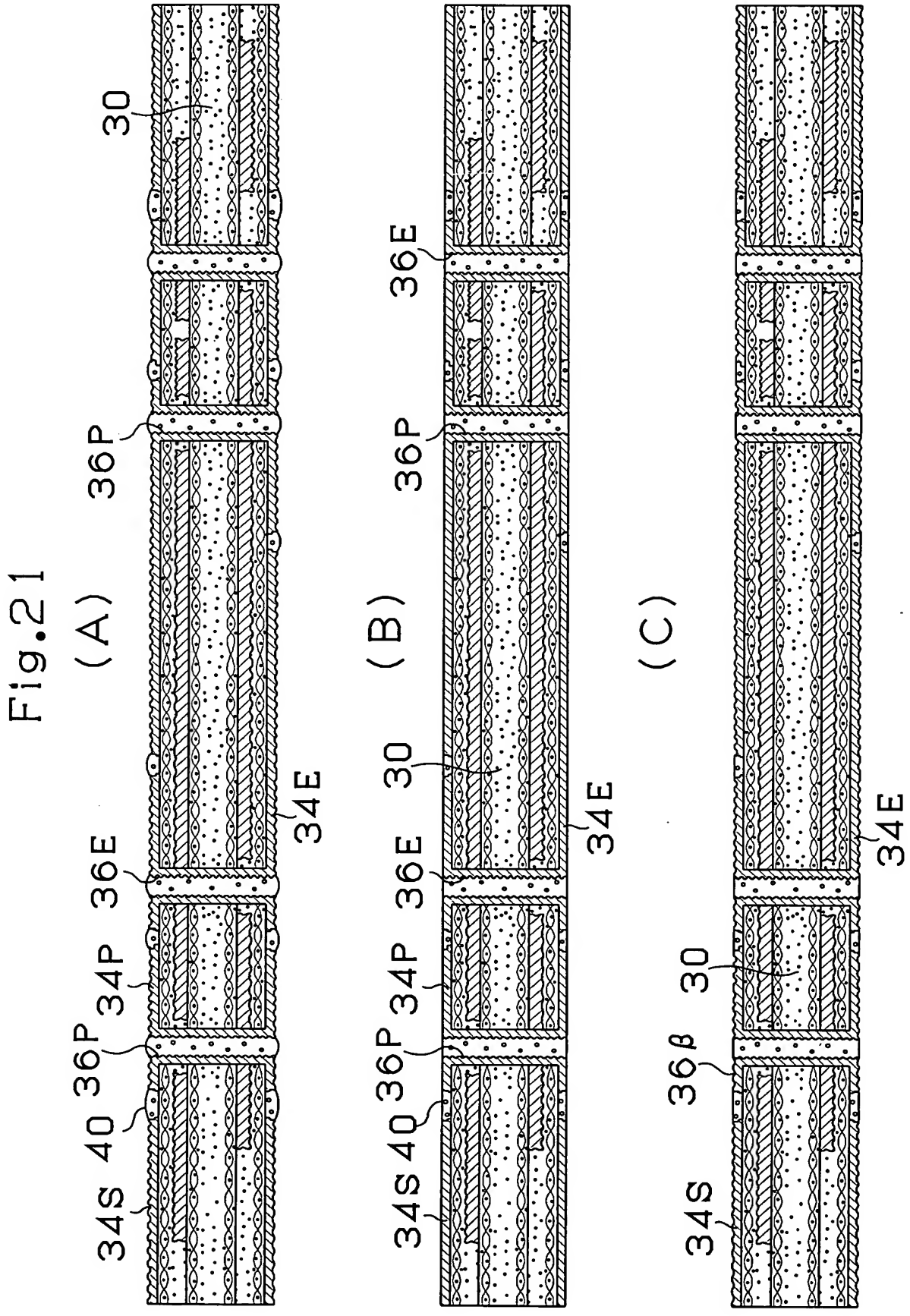

(A)
30
36
20
20
(B)
36E
30
36P
34E
36E
34P
36P
34S
(C)
36E
30
36P
34β
34E
36E
34P
36P
34S

Fig.21


(A)
30
36P
36E
34E
34P
36P
40
34S
(B)
36E
30
34E
36E
34P
36P
40
34S
(C)
30
36β
34S
34E

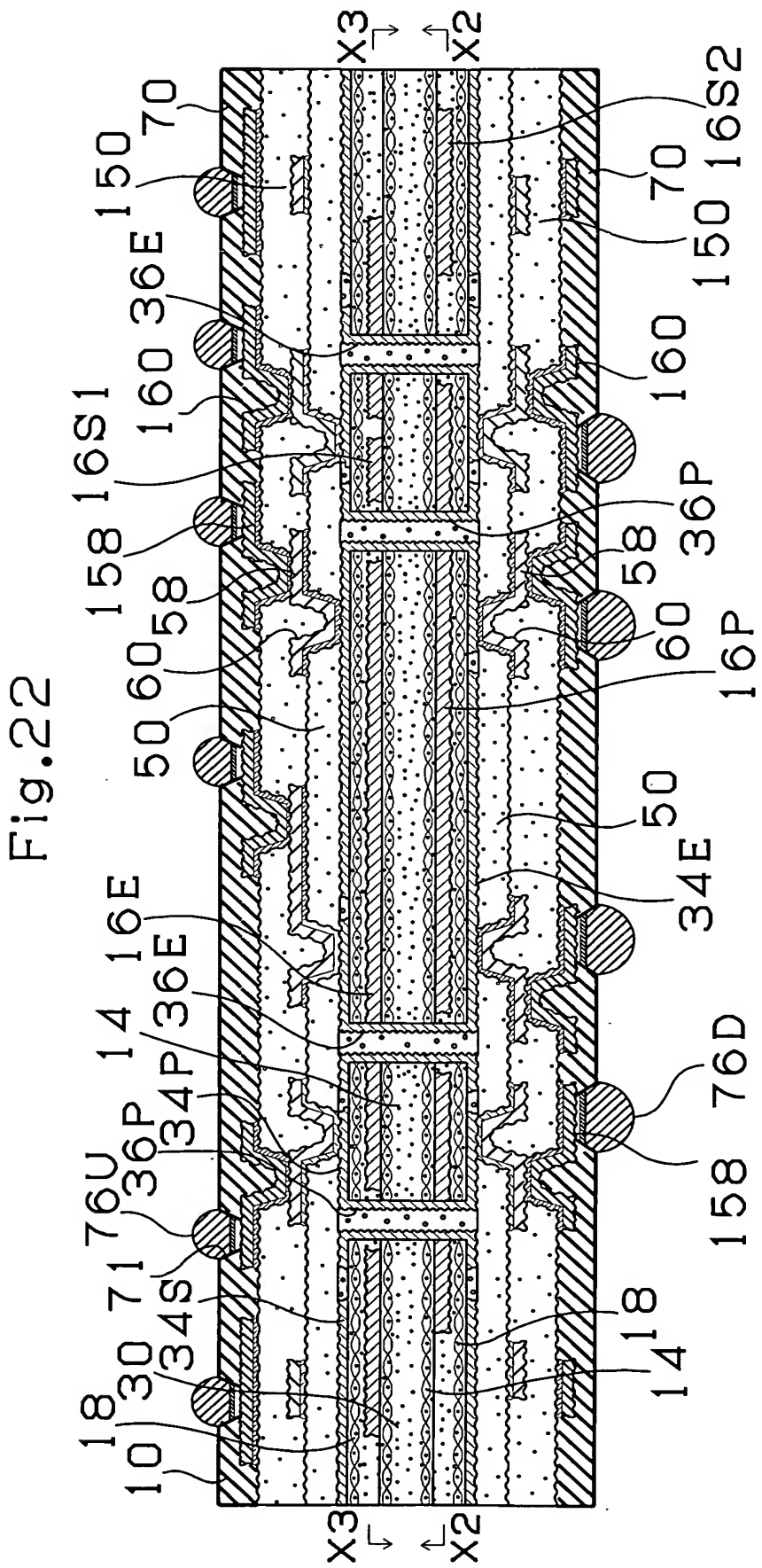

X3
X2
70
150
36E
160
16S1
158
58
60
50
16E
14
36E
34P
36P
76U
71
34S
30
18
10
16S2
70
150
160
36P
58
60
16P
50
34E
76D
158
18
14
X3
X2

Fig.22

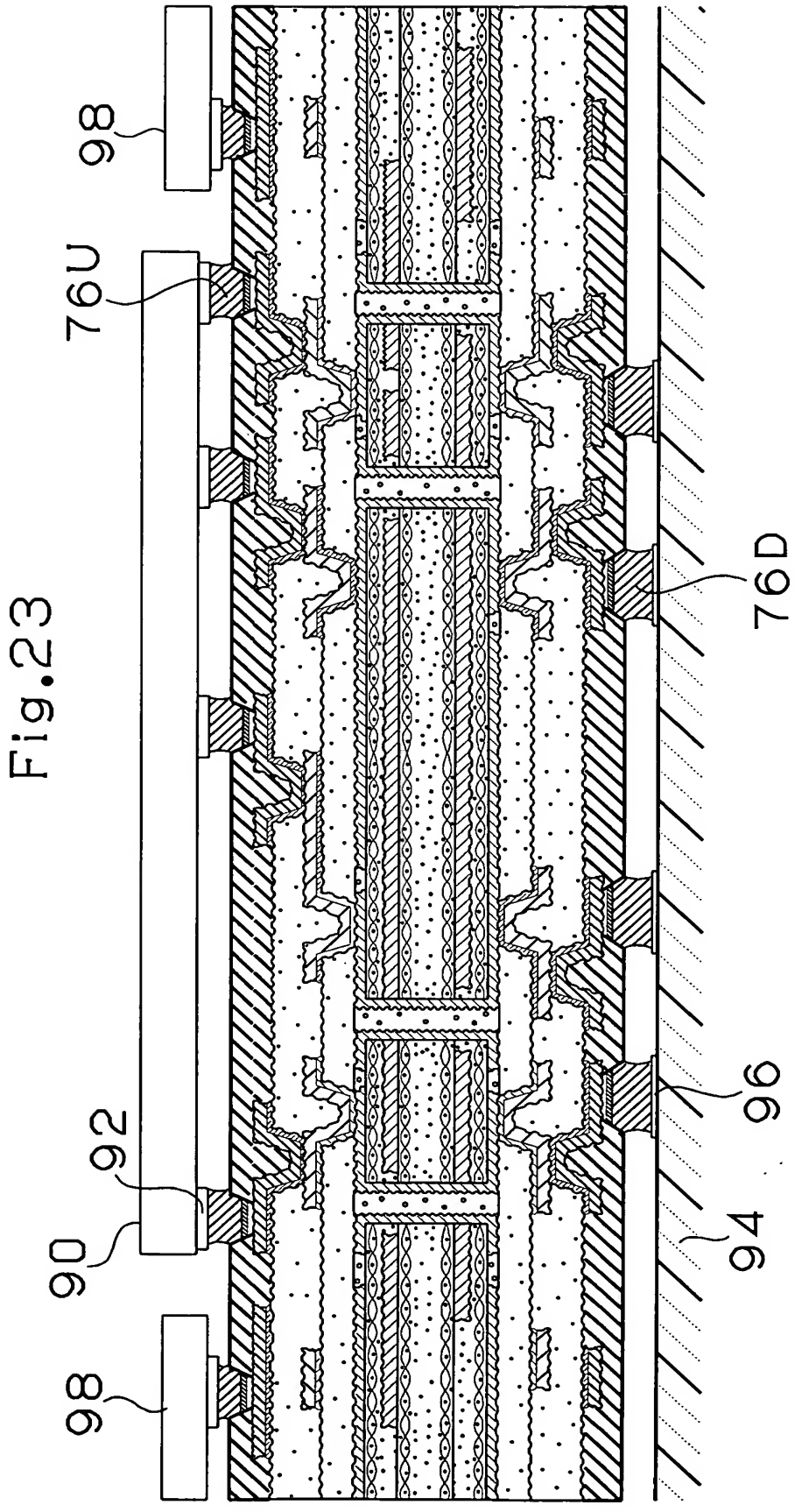


Fig.23

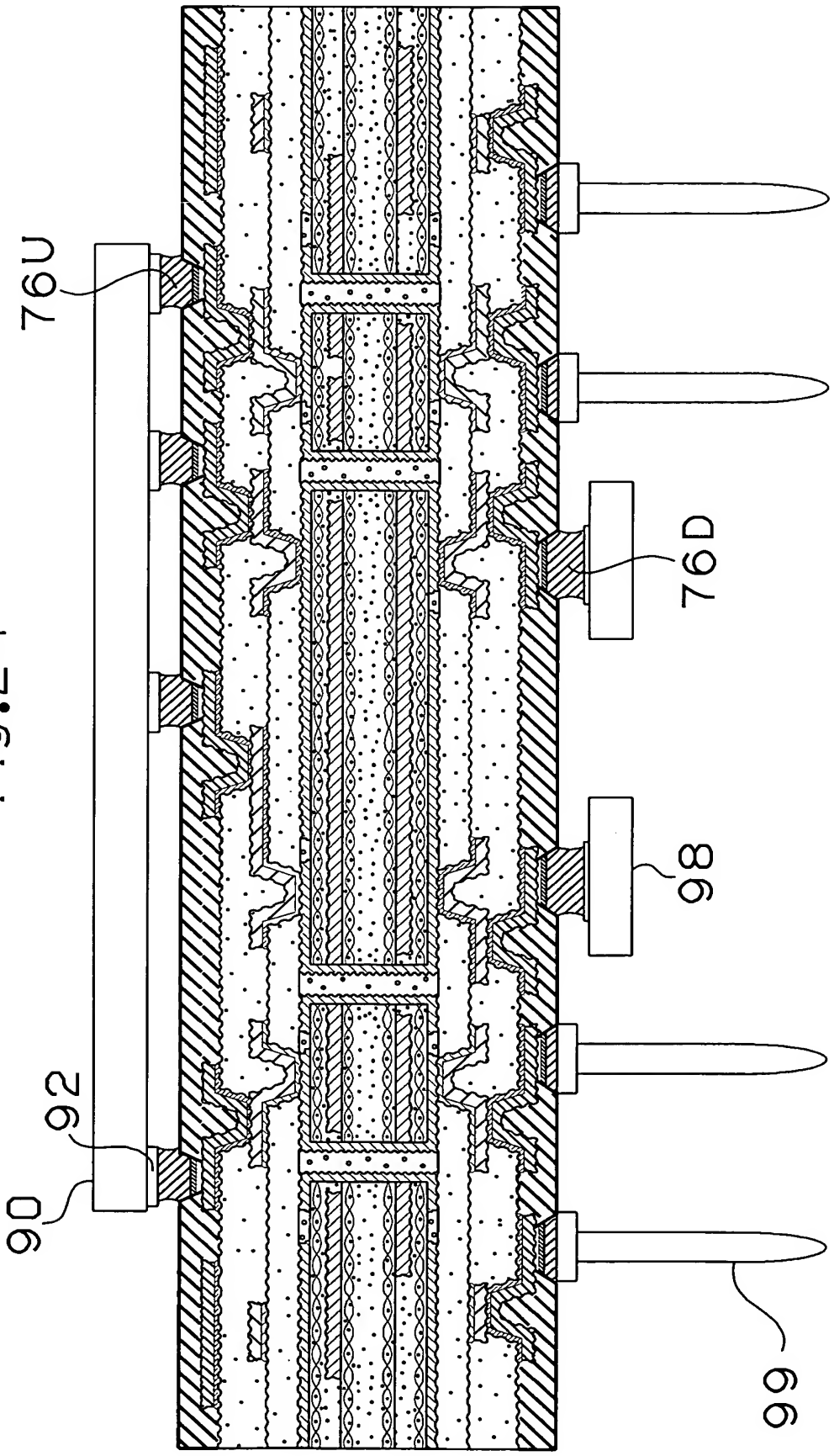


Fig.24

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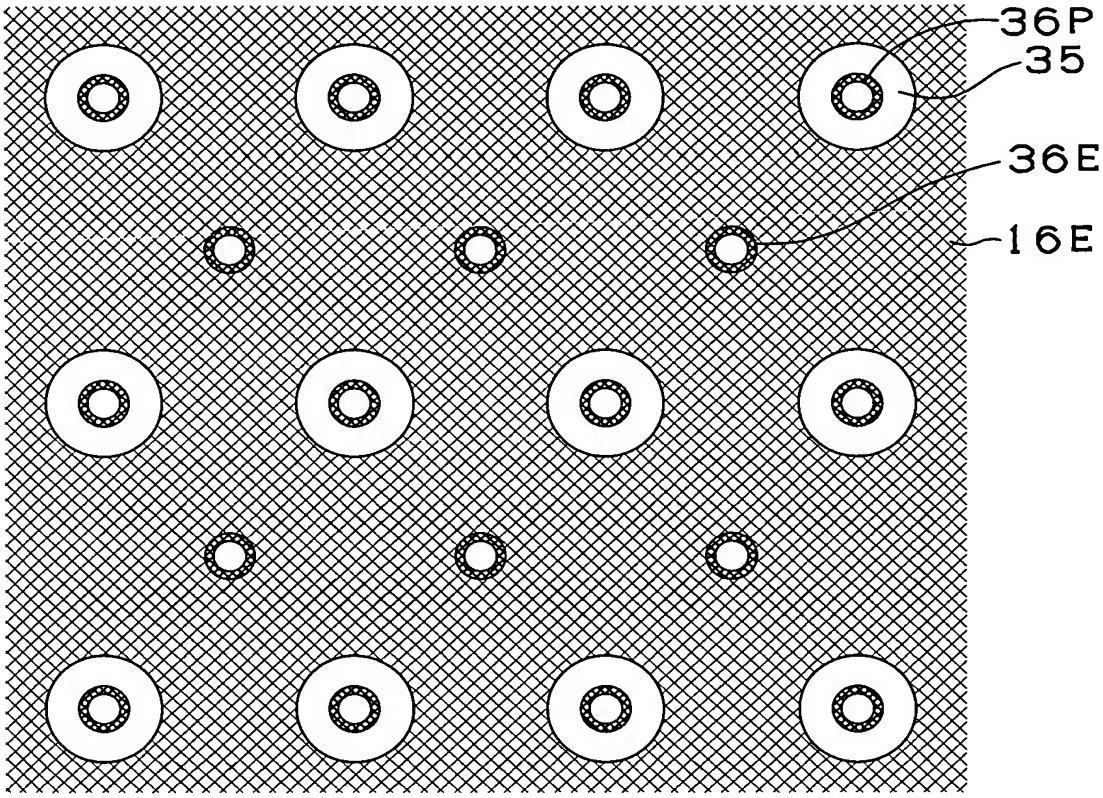
Fig.25

(A)



(B)

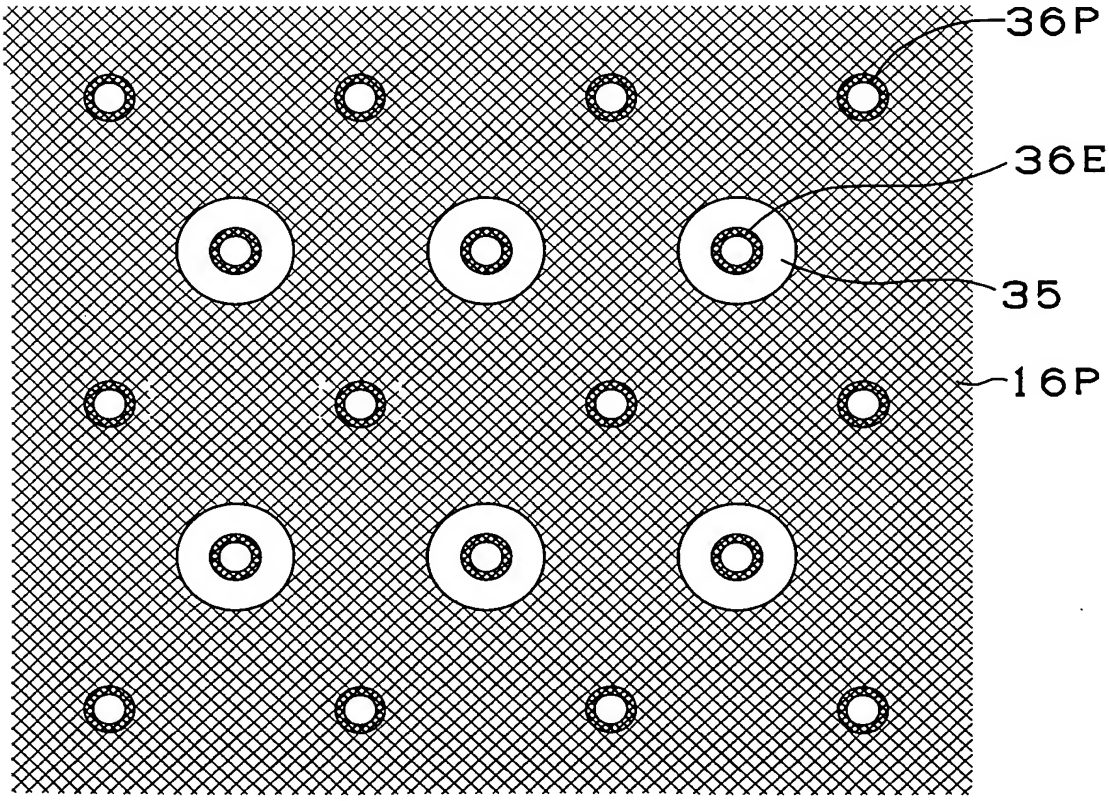


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Fig.26

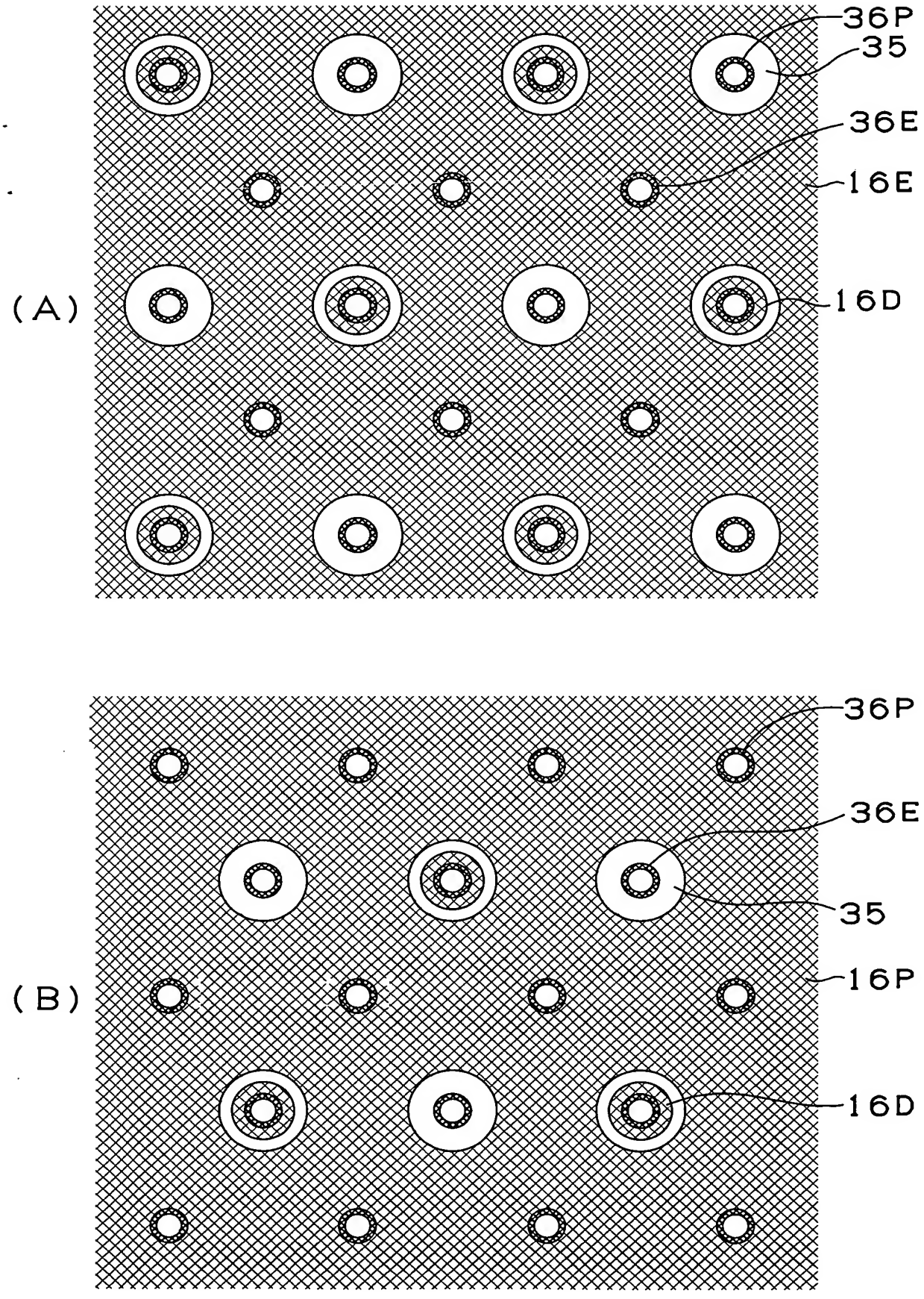


Fig.27

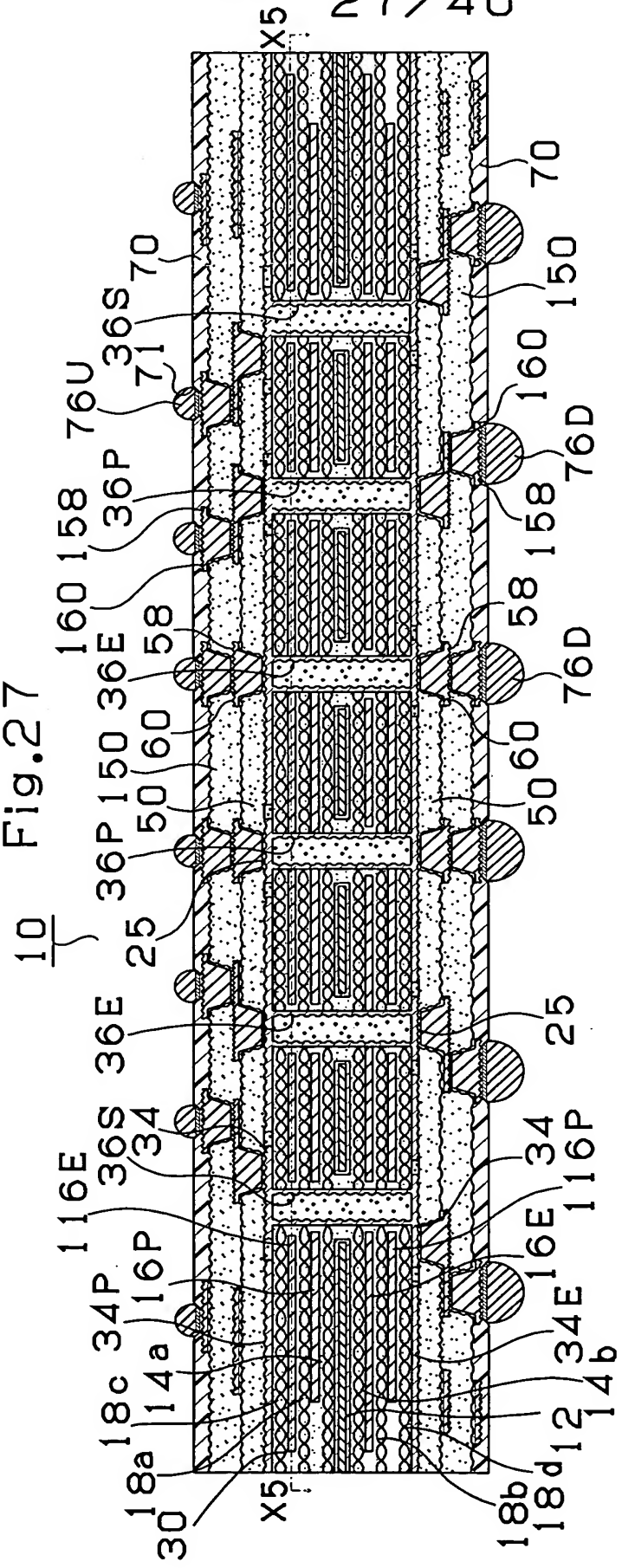

X5
70
150
36S
71
76U
160
76D
36P
158
58
36E
60
50
25
116E
34
116P
16P
34P
16E
34E
18c
14a
14b
18a
12
18d
30
18b

Fig.28

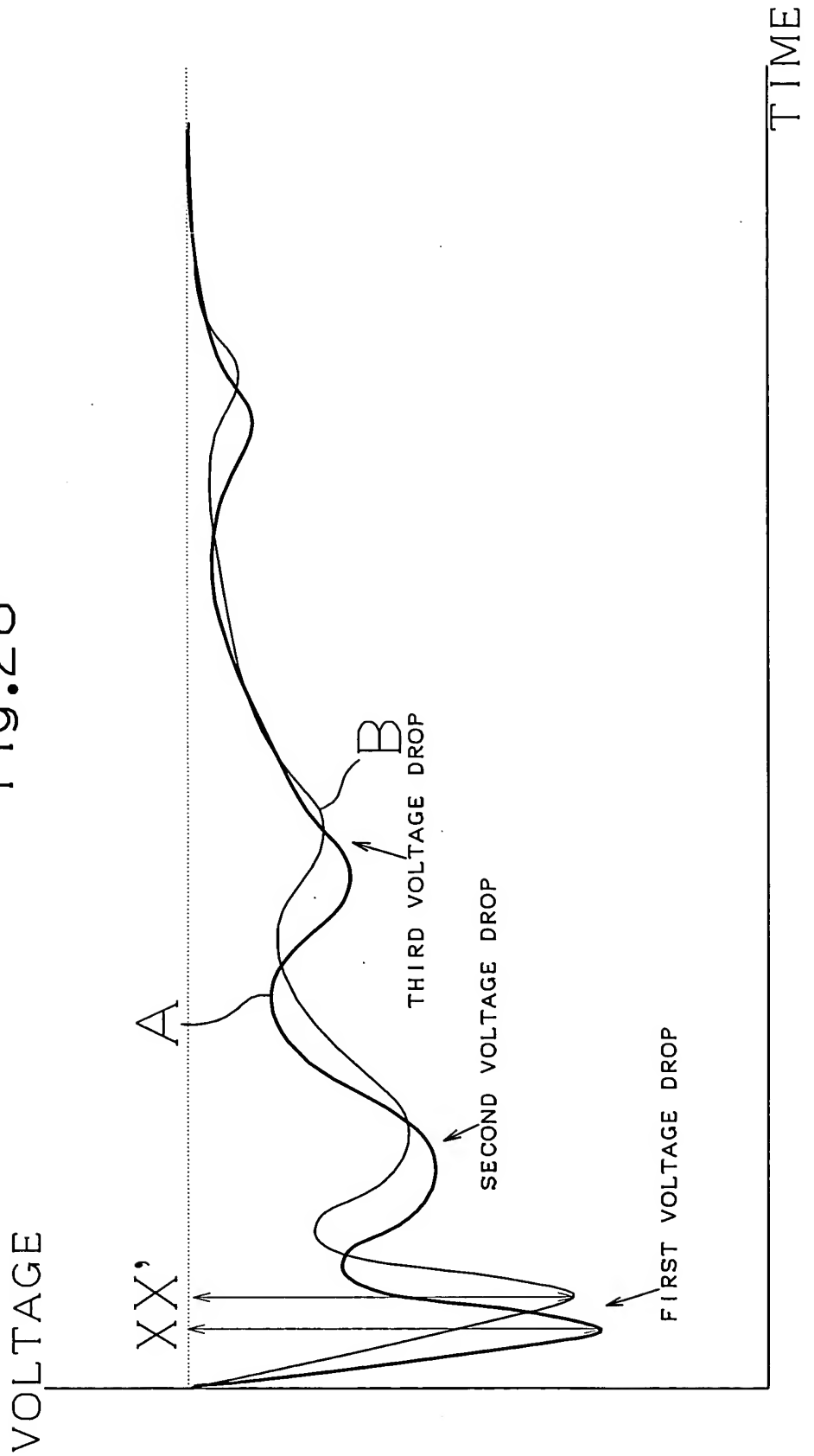

VOLTAGE
TIME
XX'
A
B
THIRD VOLTAGE DROP
SECOND VOLTAGE DROP
FIRST VOLTAGE DROP

Fig.29

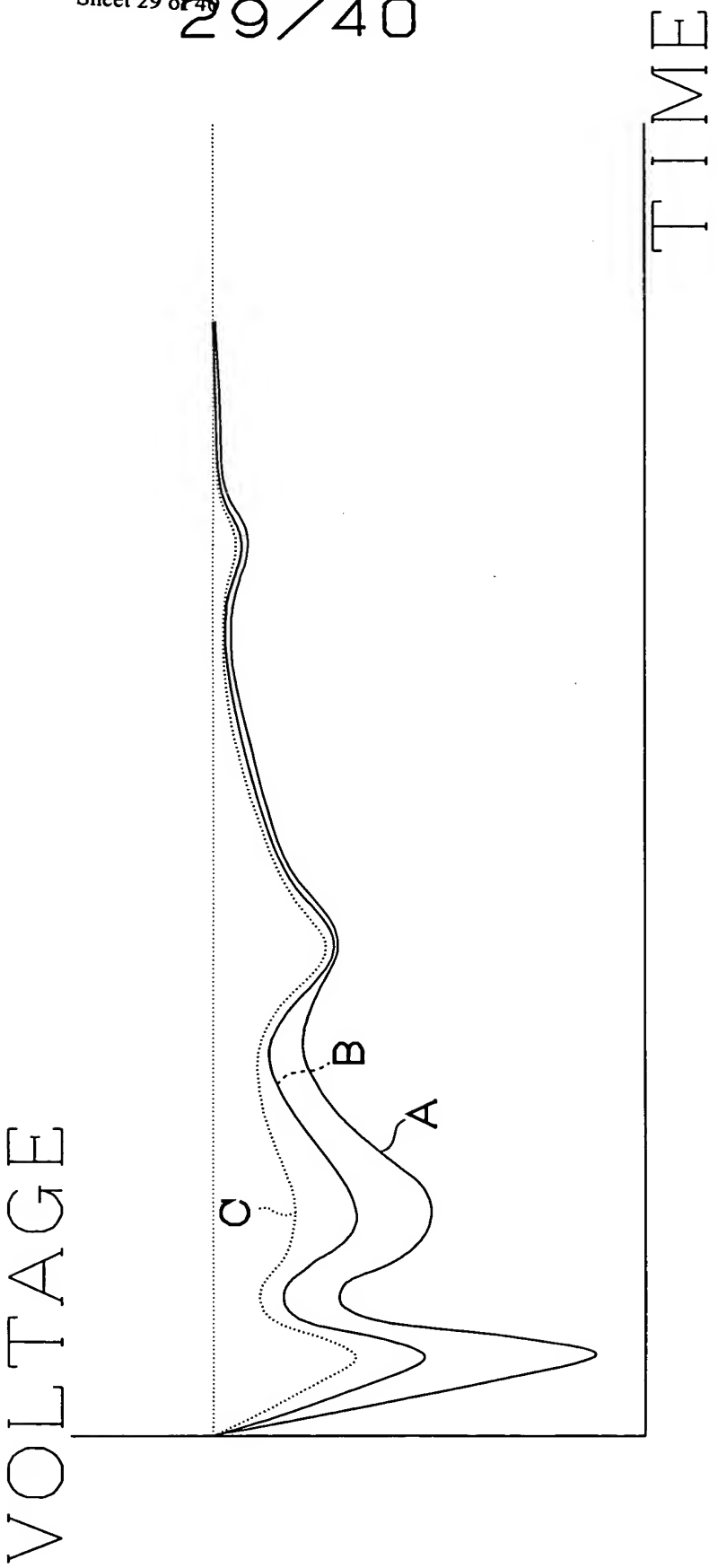
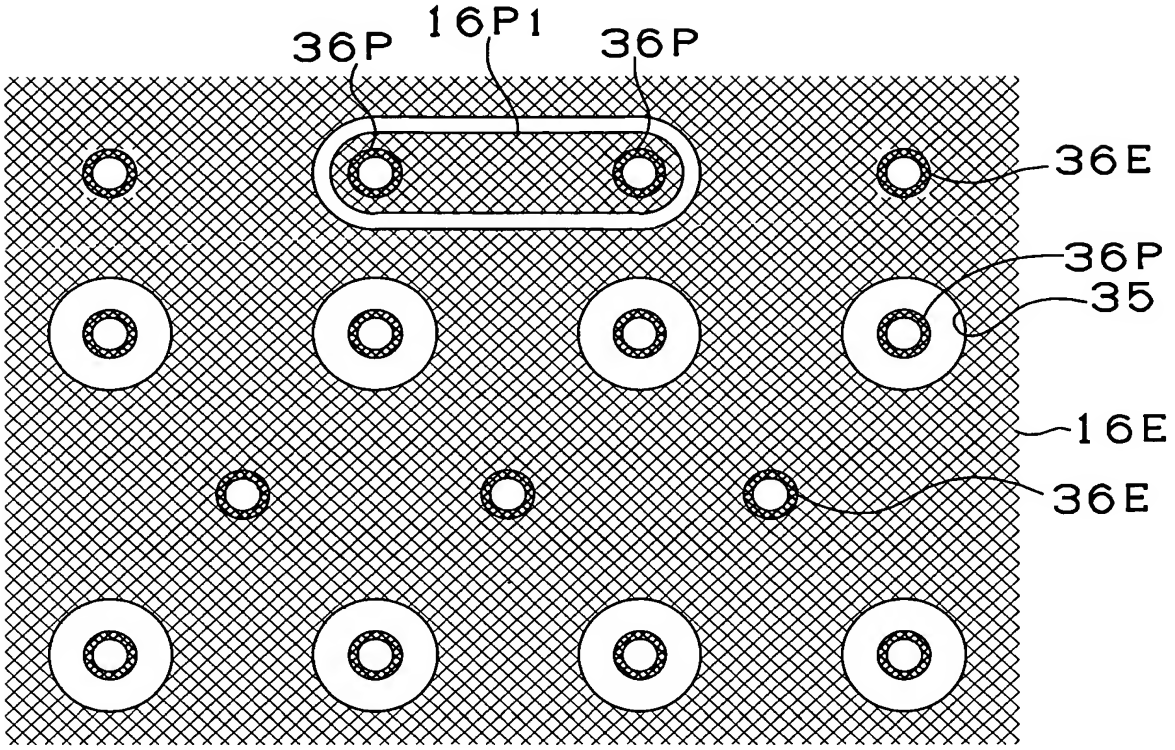


Fig.30

#	THICKNESS OF CONDUCTOR OF BU LAYER (μm)	THICKNESS OF CONDUCTOR IN INNER LAYER OF MULTILAYER CORE (μm)	REGION HAVING NO DUMMY LAND OR/AND PERCENTAGE THEREOF	AMOUNT OF VOLTAGE DROP (V)			PRESENCE/ABSENCE OF IC MALFUNCTION		
				FIRST TIME	SECOND TIME	THIRD TIME	#1(3. 06 GHz400MHz)	#2(3. 2 GHz,800MHz)	#3 (3.46GHz,1066MHz)
SECOND EMBODIMENT-11	15	30	JUST BELOW IC	0.154	0.116	0.086	NONE	NONE	YES
SECOND EMBODIMENT-12	15	30	50%	0.222	0.132	0.086	NONE	YES	YES
SECOND EMBODIMENT-13	15	30	70%	0.206	0.128	0.086	NONE	NONE	YES
SECOND EMBODIMENT-14	15	30	80%	0.202	0.126	0.087	NONE	NONE	YES
SECOND EMBODIMENT-15	15	30	90%	0.205	0.122	0.085	NONE	NONE	YES
SECOND EMBODIMENT-16	15	45	JUST BELOW IC	0.137	0.108	0.078	NONE	NONE	NONE
SECOND EMBODIMENT-17	15	60	JUST BELOW IC	0.135	0.108	0.076	NONE	NONE	NONE
SECOND EMBODIMENT-18	15	75	JUST BELOW IC	0.130	0.106	0.074	NONE	NONE	NONE
SECOND EMBODIMENT-19	15	75	70%	0.132	0.106	0.074	NONE	NONE	NONE
SECOND EMBODIMENT-20	15	45	30% JUST BELOW	0.201	0.123	0.078	NONE	NONE	YES
SECOND EMBODIMENT-21	15	60	30% JUST BELOW	0.159	0.118	0.076	NONE	NONE	NONE
SECOND EMBODIMENT-22	15	75	30% JUST BELOW	0.155	0.117	0.074	NONE	NONE	NONE
SECOND EMBODIMENT-23	15	150	30% JUST BELOW	0.154	0.116	0.072	NONE	NONE	NONE
SECOND EMBODIMENT-24	15	300	30% JUST BELOW	0.208	0.129	0.086	NONE	NONE	YES
SECOND EMBODIMENT-25	15	45	50% JUST BELOW	0.165	0.120	0.078	NONE	NONE	NONE
SECOND EMBODIMENT-26	15	60	50% JUST BELOW	0.155	0.117	0.076	NONE	NONE	NONE
SECOND EMBODIMENT-27	15	75	50% JUST BELOW	0.155	0.117	0.074	NONE	NONE	NONE
SECOND EMBODIMENT-28	15	150	50% JUST BELOW	0.155	0.117	0.072	NONE	NONE	NONE
SECOND EMBODIMENT-29	15	300	50% JUST BELOW	0.201	0.129	0.086	NONE	NONE	YES
SECOND EMBODIMENT-30	15	45	70% JUST BELOW	0.155	0.117	0.078	NONE	NONE	NONE
SECOND EMBODIMENT-31	15	60	70% JUST BELOW	0.155	0.117	0.076	NONE	NONE	NONE
SECOND EMBODIMENT-32	15	75	70% JUST BELOW	0.155	0.117	0.074	NONE	NONE	NONE
SECOND EMBODIMENT-33	15	150	70% JUST BELOW	0.155	0.117	0.072	NONE	NONE	NONE
SECOND EMBODIMENT-34	15	300	70% JUST BELOW	0.203	0.127	0.086	NONE	NONE	YES
SECOND EMBODIMENT-35	15	60	50%	0.201	0.130	0.078	NONE	NONE	YES
SECOND EMBODIMENT-36	15	30	50% JUST BELOW	0.204	0.121	0.078	NONE	NONE	YES
SECOND COMPARATIVE EXAMPLE-3	15	5	NONE	0.306	0.150	0.087	YES	YES	YES

Fig.31

(A)



(B)

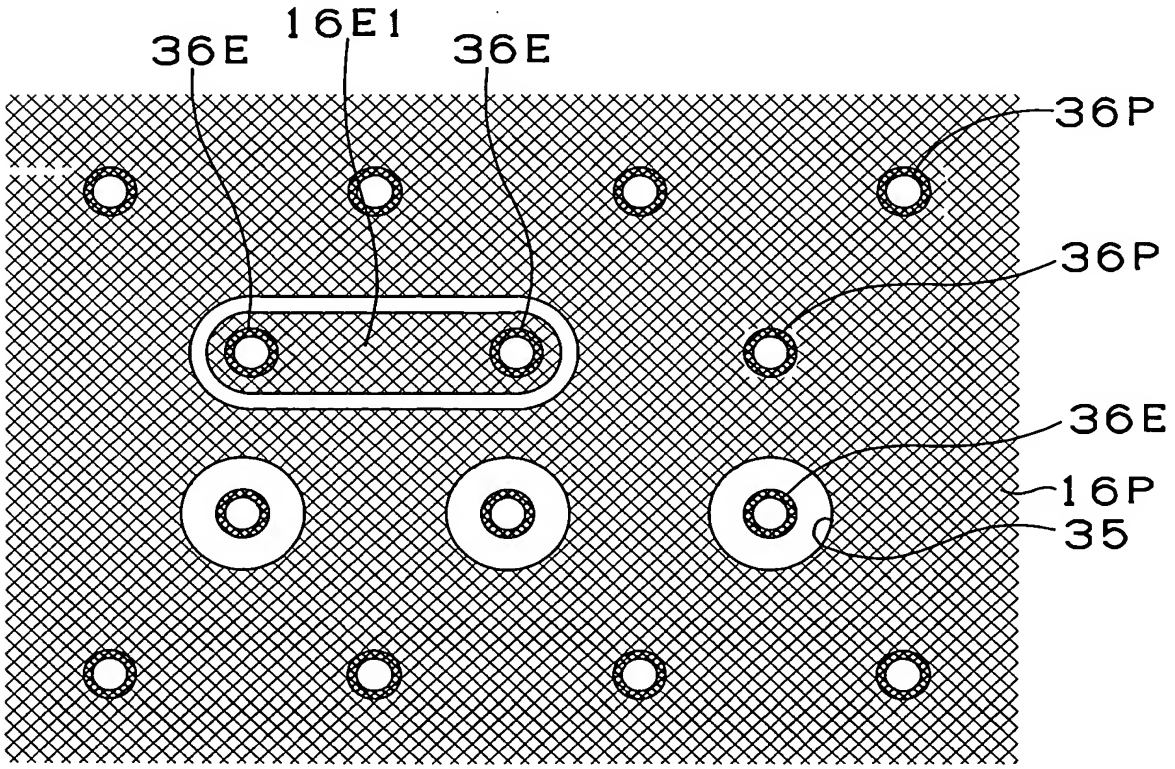


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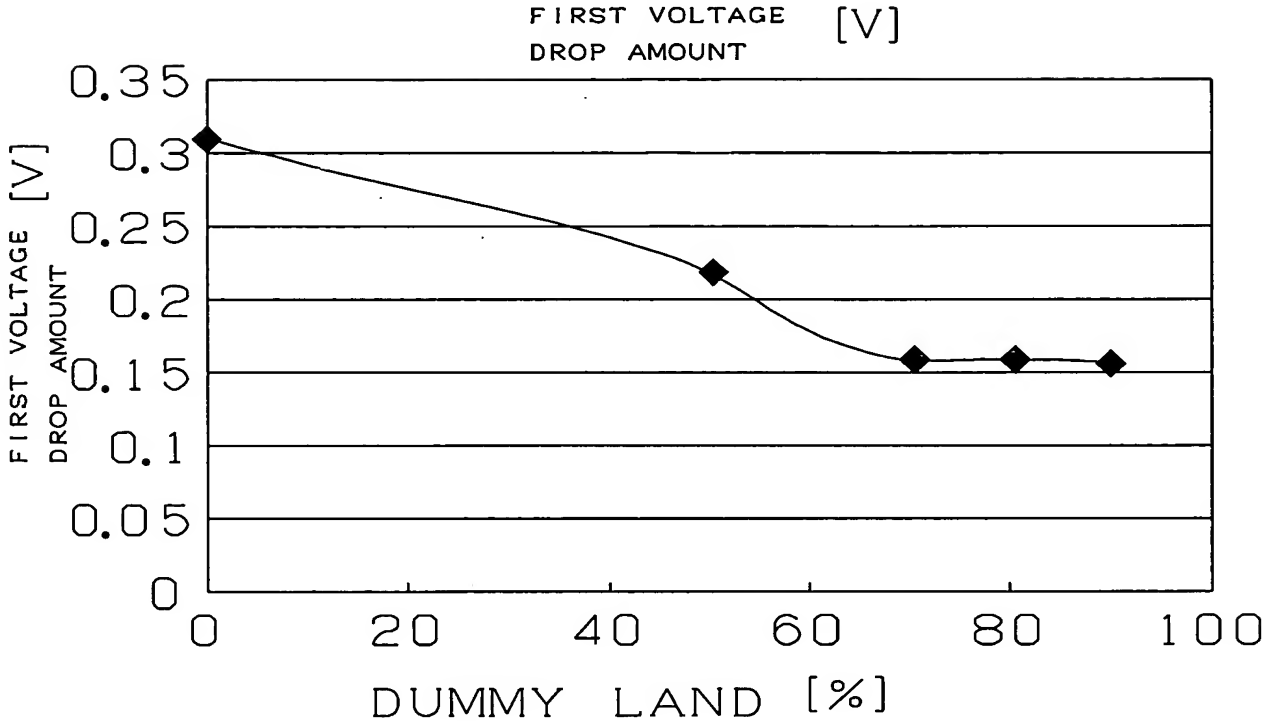
Fig.32

(A)



(B)

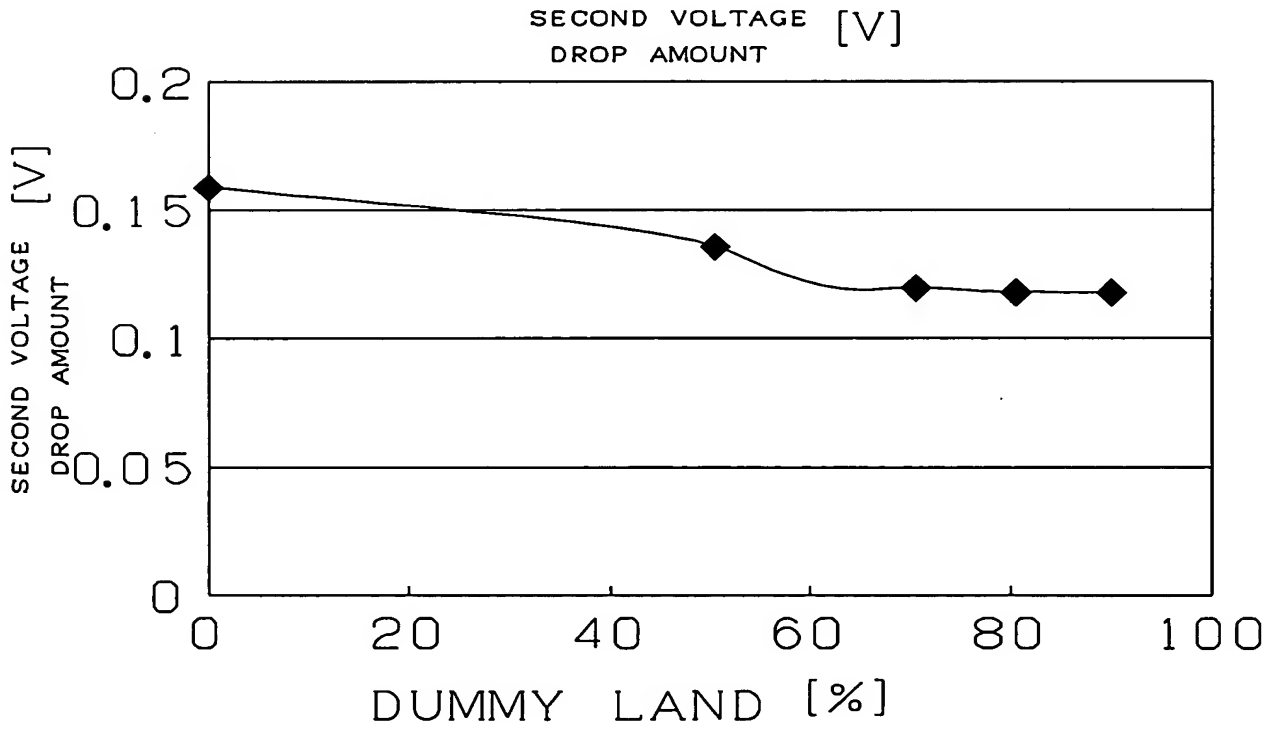


Fig.33

#	THICKNESS OF Cu IN BUILT-UP LAYER (μm)	THICKNESS OF Cu IN INNER LAYER OF MULTILAYER CORE (μm)	RESION HAVING NO DUMMY LAND OR PERCENTAGE THEREOF	AMOUNT OF VOLTAGE DROP(V)			PRESENCE/ ABSENCE OF IC MALFUNCTION
				FIRST TIME	SECOND TIME	THIRD TIME	
SECOND EMBODIMENT1	15	30	JUST BELOW IC	0. 157	0. 118	0. 089	NONE
SECOND EMBODIMENT2	15	30	50%	0. 218	0. 135	0. 088	YES
SECOND EMBODIMENT3	15	30	70%	0. 158	0. 120	0. 088	NONE
SECOND EMBODIMENT4	15	30	80%	0. 158	0. 118	0. 089	NONE
SECOND EMBODIMENT5	15	30	90%	0. 155	0. 118	0. 087	NONE
SECOND EMBODIMENT6	15	45	JUST BELOW IC	0. 140	0. 110	0. 088	NONE
SECOND EMBODIMENT7	15	60	JUST BELOW IC	0. 138	0. 110	0. 088	NONE
SECOND EMBODIMENT8	15	75	JUST BELOW IC	0. 133	0. 108	0. 086	NONE
SECOND EMBODIMENT9	15	75	70%	0. 135	0. 108	0. 086	NONE
SECOND COMPARATIVE EXAMPLE1	15	30	NONE	0. 310	0. 153	0. 089	YES
SECOND COMPARATIVE EXAMPLE2	15	15	NONE	0. 389	0. 160	0. 108	YES

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Fig.34

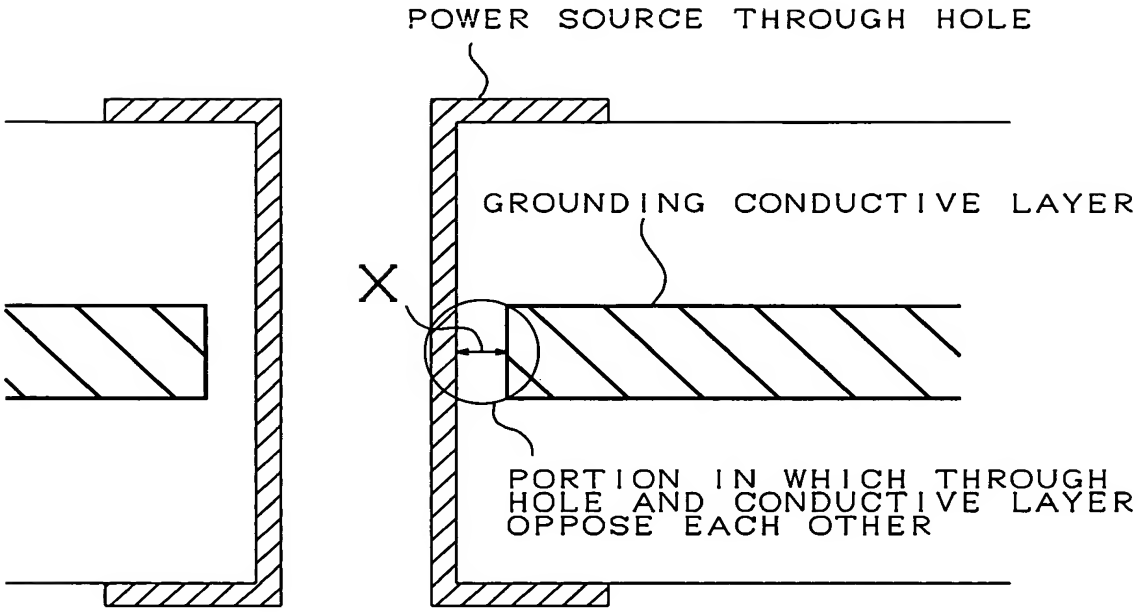
POWER SOURCE THROUGH HOLE
GROUNDING CONDUCTIVE LAYER
X
PORTION IN WHICH THROUGH HOLE AND CONDUCTIVE LAYER OPPOSE EACH OTHER

Fig.35

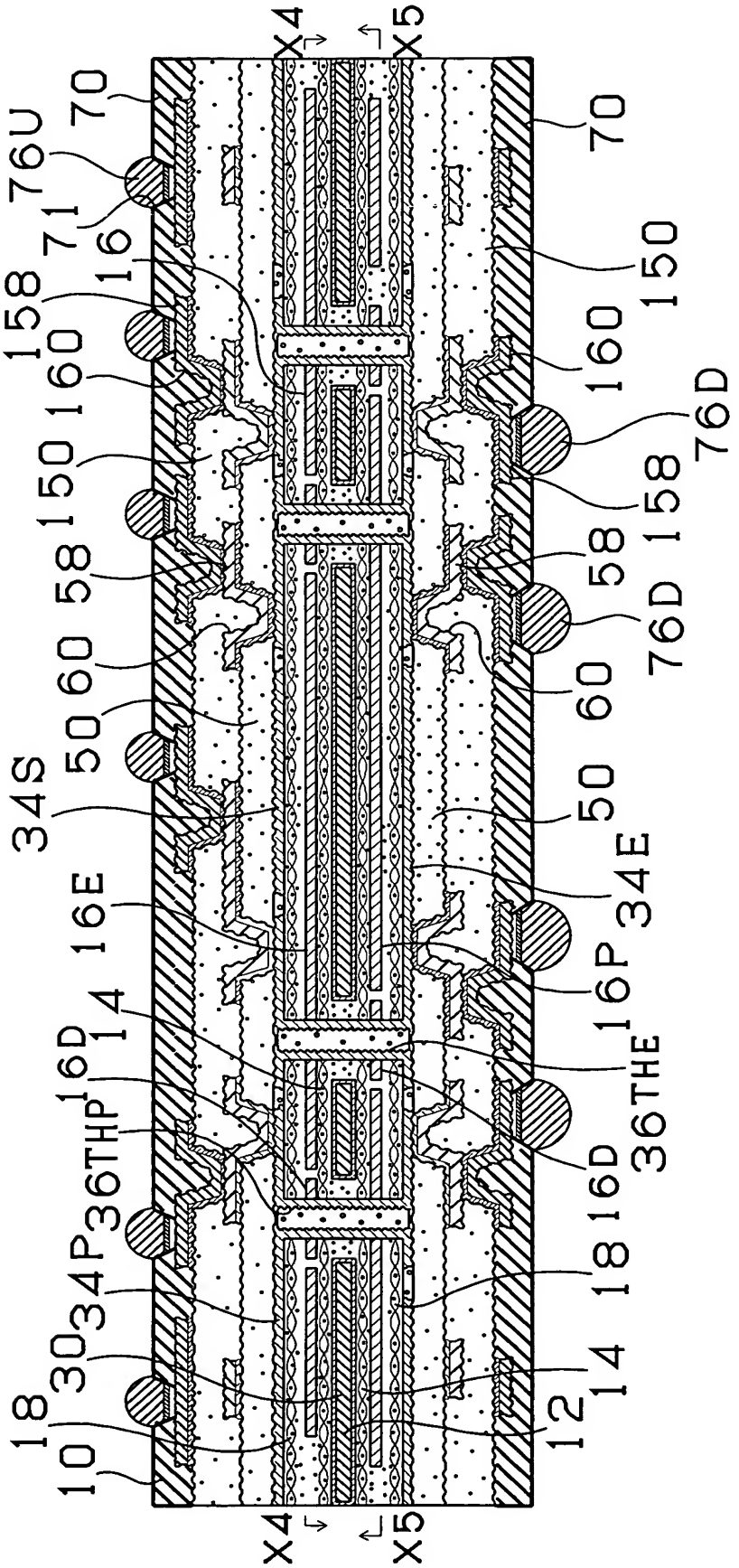
X4
X5
70
76U
71
16
158
160
150
58
60
50
34S
16E
14
16D
36THP
34P
30
18
10
12
18
14
16D
36THE
16P
34E
50
60
58
158
76D
150
160
70

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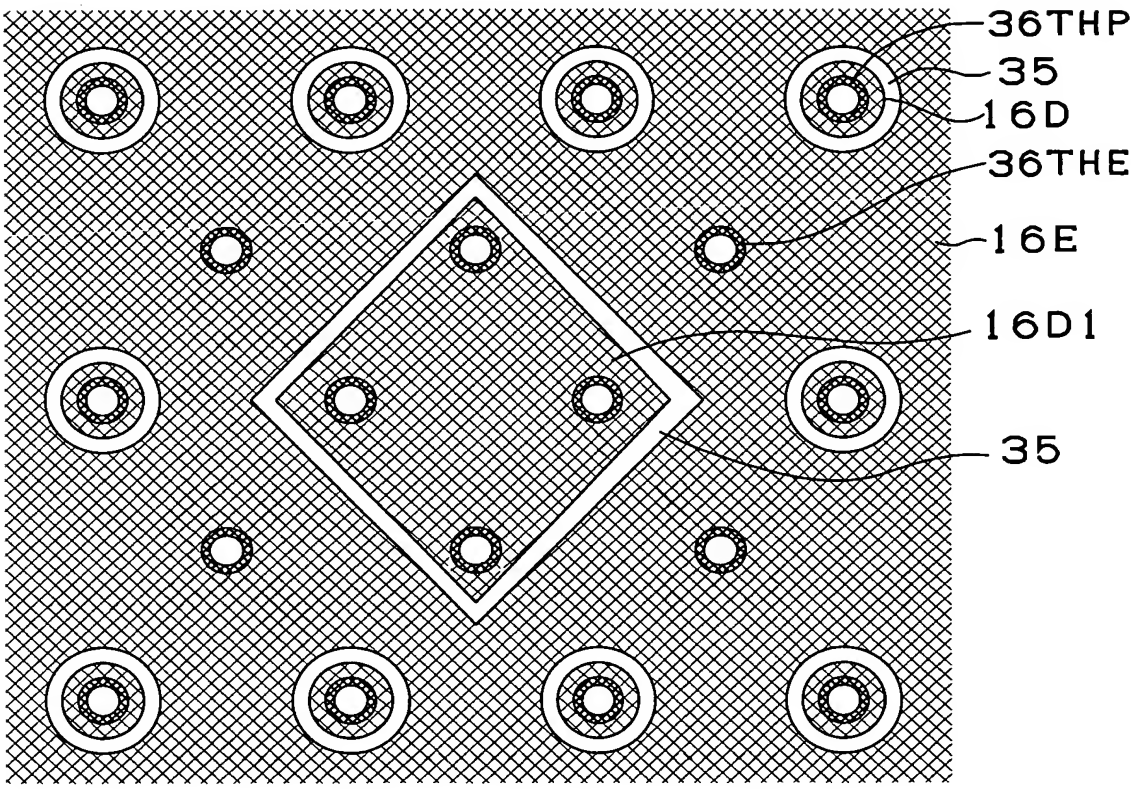
Fig.36

(A)



(B)

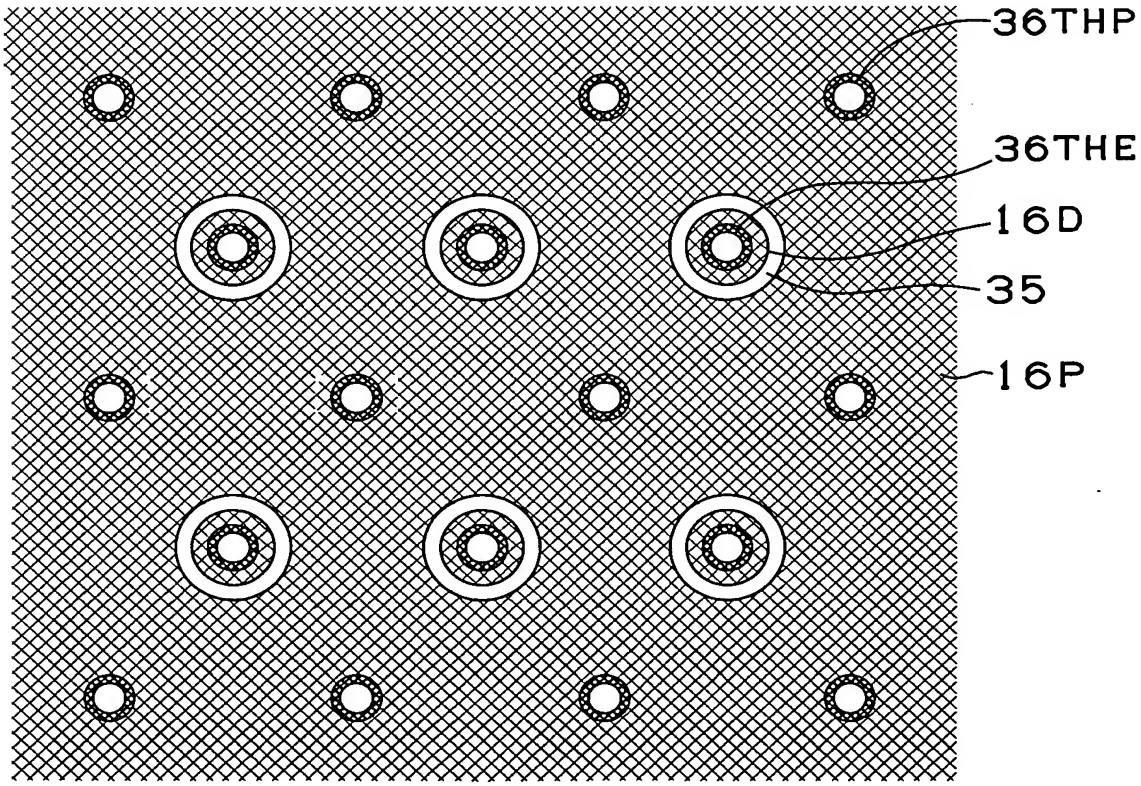


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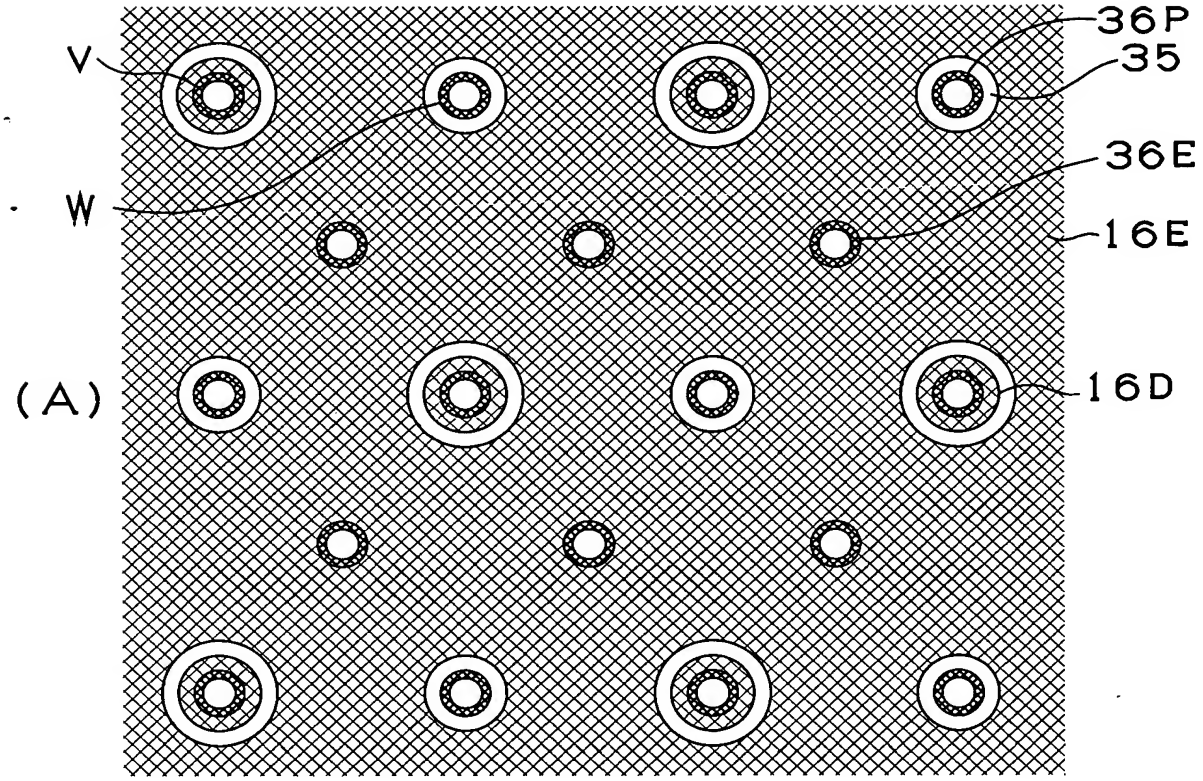
Fig.37



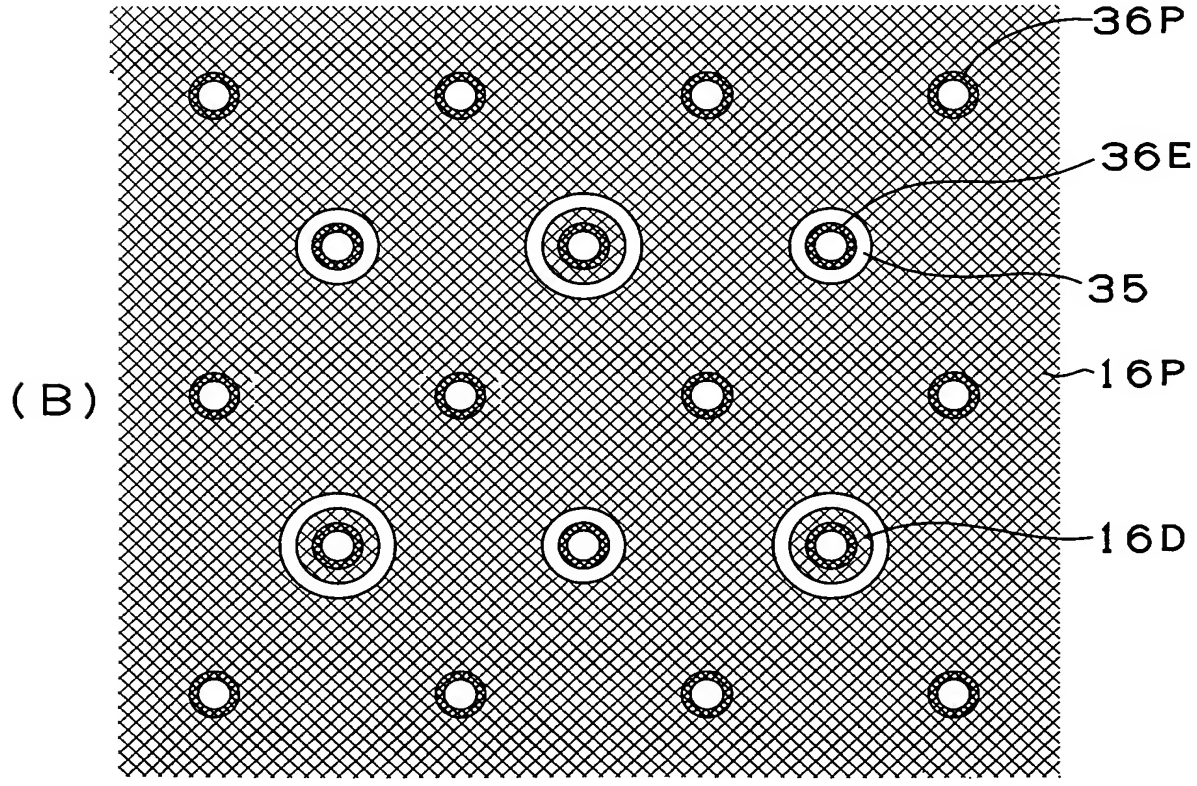


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Fig.38

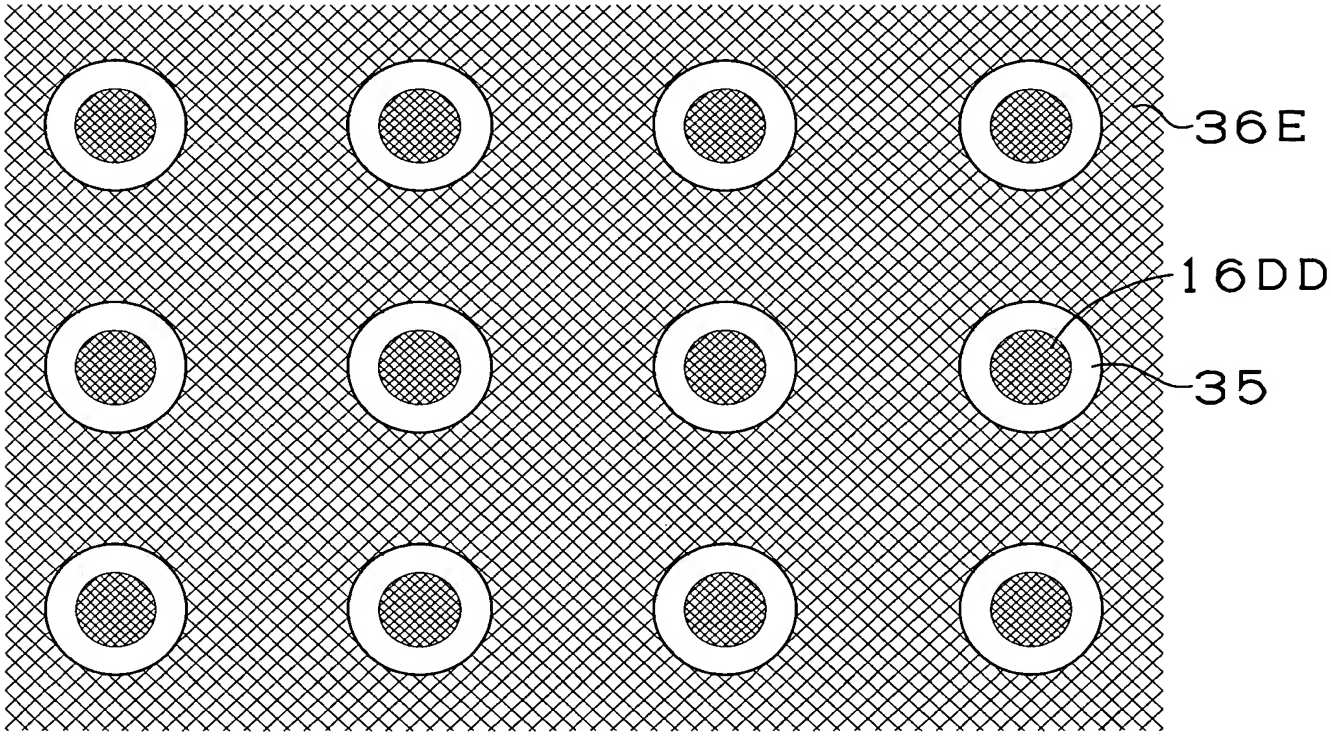

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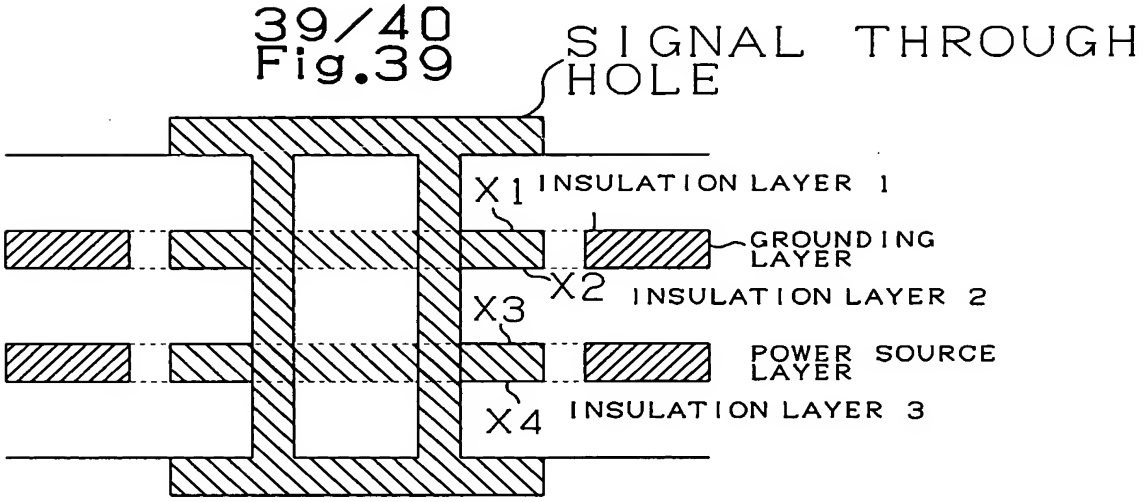
Fig.39


SIGNAL THROUGH HOLE
X1
INSULATION LAYER 1
GROUNDING LAYER
X2
INSULATION LAYER 2
X3
POWER SOURCE LAYER
X4
INSULATION LAYER 3

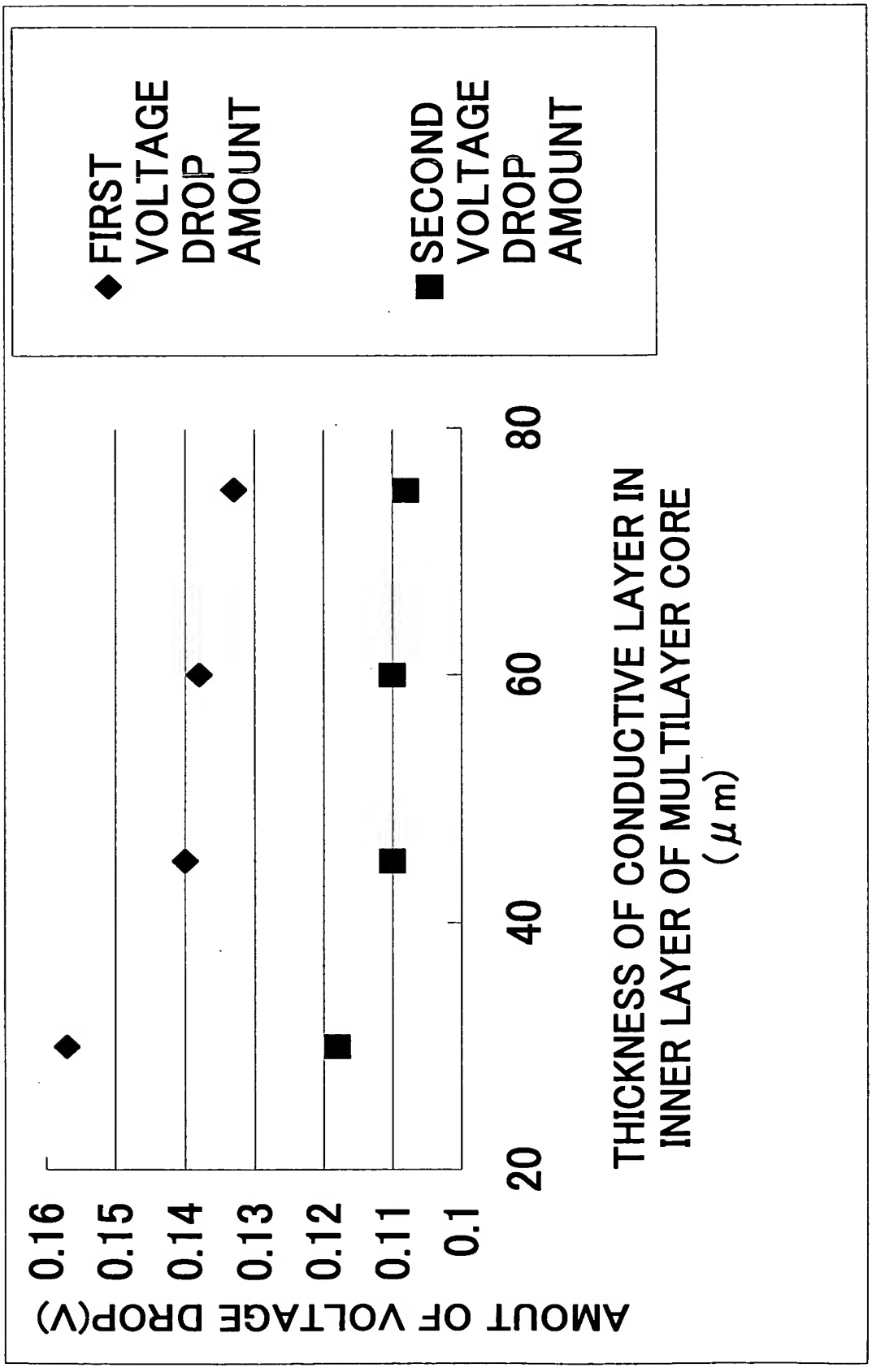

AMOUT OF VOLTAGE DROP(V)
0.16
0.15
0.14
0.13
0.12
0.11
0.1
20
40
60
80
THICKNESS OF CONDUCTIVE LAYER IN INNER LAYER OF MULTILAYER CORE (μm)
◆FIRST VOLTAGE DROP AMOUNT
■SECOND VOLTAGE DROP AMOUNT

Fig.40